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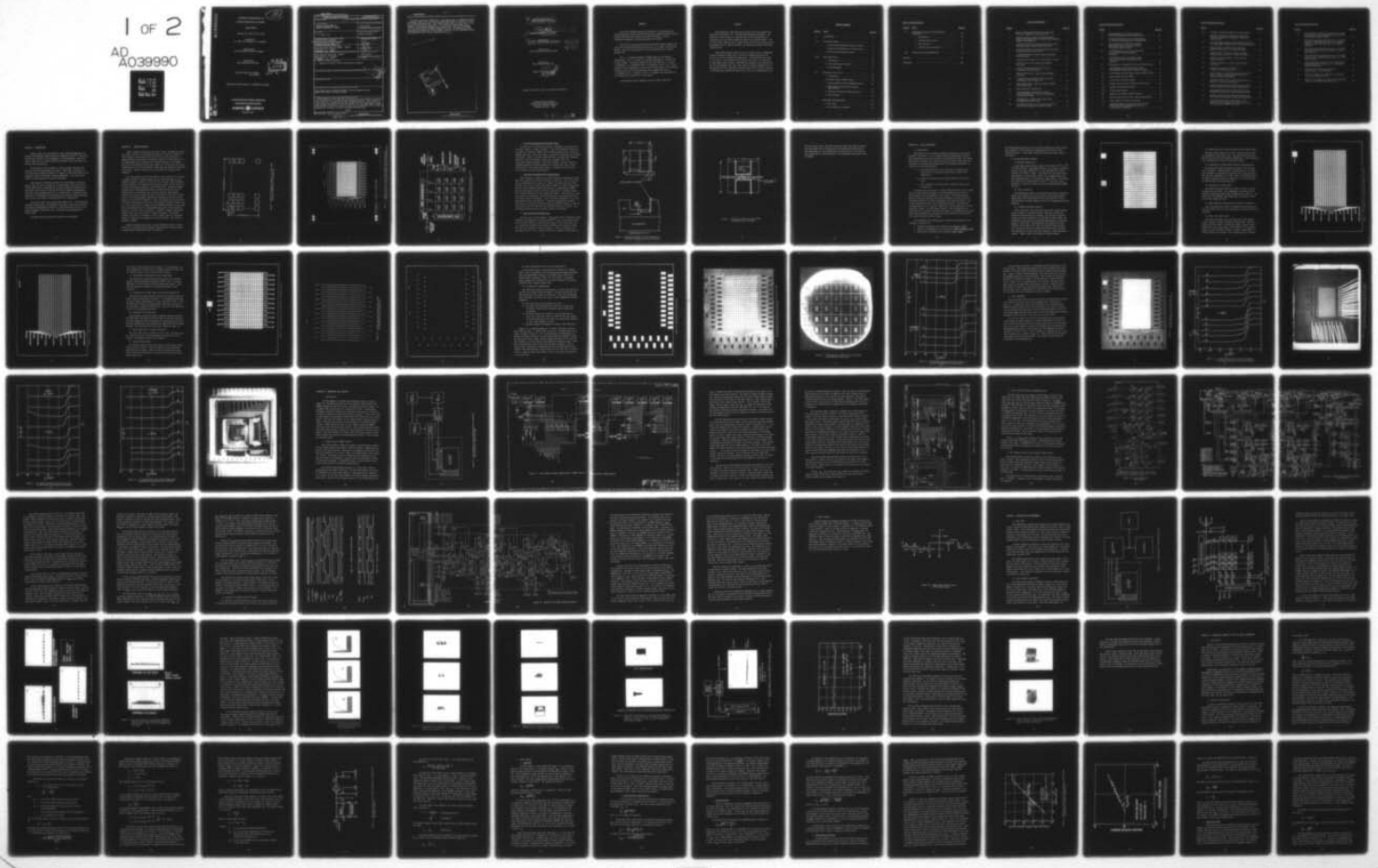

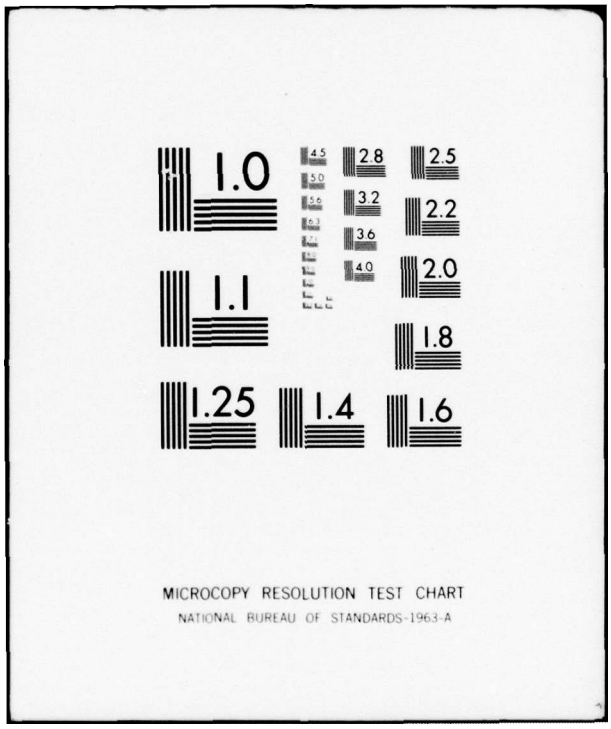
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CONTINUED DEVELOPMENT OF

INDIUM ANTIMONIDE CID ARRAYS

FINAL REPORT

Contract No. N00173-76-C-0128

Prepared by:
J.C. Kim, W.E. Davern, D. Colangelo

Sponsored by:
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Two-dimensional 16x24 InSb CID area arrays have been designed and successfully fabricated via a multilayer MIS processing technique. The operation of these arrays in a staring mode has been demonstrated by displaying real time raster-scanned IR images on an X-Y CRT monitor. The raw video image displays were as sharp as the actual objects, being clearly recognizable with no sign of blooming and, therefore, excellent operating characteristic.

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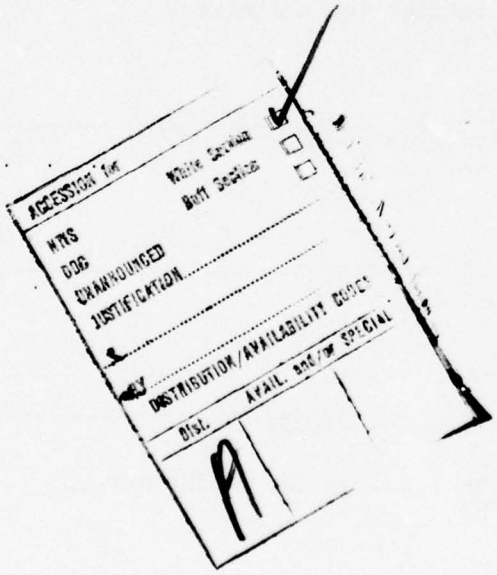

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FOREWORD

This Final Technical Report was prepared by the Optoelectronic Systems Operation of Electronic Systems Division, General Electric Company, Syracuse, New York under Contract No. N00173-76-C-0128, entitled "Continued Development of Indium Antimonide CID Arrays".

This effort was sponsored by Naval Electronic Systems Command, and directed by Naval Research Laboratory with Dr. W. D. Baker as the Project Monitor. The work was performed for the period October 1975 through October 1976.

Mr. L. A. Branaman, Manager of Engineering, was the Program Administrator. Dr. J. C. Kim, the Principal Investigator, directed the overall program. The array process work was performed by W. E. Davern, T. Shepelavy, V. F. Meikleham and E. M. Littebrant, and Mr. W. E. Davern assisted in the preparation of Section III of this report. The electronic circuits used for the array evaluation were designed and built by D. Colangelo and R. J. Schultz, and Mr. D. Colangelo was responsible for the preparation of Section IV of this report.

Distribution of this technical report was made in May 1977.

ABSTRACT

Two-dimensional 16x24 InSb CID area arrays have been designed and successfully fabricated via a multilayer MIS processing technique. The operation of these arrays in a staring mode has been demonstrated by displaying real time raster-scanned IR images on an X-Y CRT monitor. The raw video image displays were as sharp as the actual objects, being clearly recognizable with no sign of blooming, and exhibiting excellent operating characteristics.

Theoretical analysis showed that at low sample rates, a background limited performance (BLIP) can be obtained at background photon flux levels of as low as mid-10^{12} photons/sec-cm^2. The dominant noise source, in this case, is the integrated dark current shot noise. For operation at high sample rates, however, the bandwidth-dependent noise sources limit the array performance and, thus, BLIP occurs at higher background levels. The analysis has been confirmed by measured data on line arrays, resulting in good agreement between the theoretical curve and the experimental data.

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SECTION I. INTRODUCTION

Single column, 1x16 arrays based on the InSb MIS technology, were designed and fabricated under Contract No. N00014-75-C-0124[1]. This work has now been extended to the development of two-dimensional, 16x24 area arrays, which are to be used as focal plane arrays in time delay and integration (TDI) applications.

The objective of this program is, then, to design, fabricate and evaluate 16x24 two-dimensional area arrays. Each array is operated via two silicon shift-register scanners, by reading out the video signal in the sequential raster scan through a common preamplifier. The output video signal is then displayed on a scope or CRT screen.

This program is primarily devoted to the development of InSb CID arrays; there has been no attempt to interface these arrays with Si CCD for TDI applications. Nevertheless, we have developed an appropriate two-dimensional array structure that has been used to generate recognizable, real-time, raster-scanned images on an x-y CRT monitor. Eventually these arrays will be incorporated in scanning systems with TDI signal processing but, for now, the arrays are being evaluated in a staring mode.

This final report covers mask design (Section II). The fabrication procedure (Section III), the associated electronic circuitry (Section IV), evaluation and measurements (Section V), the theoretical analysis of the array performance (Section VI), and, conclusions and recommendations (Section VII).

Pertinent device data has been included in the Appendix.

SECTION II. ARRAY MASK DESIGN

Figure 1 shows the layout for the 16x24 arrays, including the active unit cells. The size of the resolution element is 2x2 mils, located on 3-mil centers in one direction and 2.6 mils in the other direction. A complete layout of the array is presented in Figure 2, which shows all of the bonding pads for the silicon shift register scanners. The bonding pads for the 16-element side have been fanned out to facilitate wire interconnections; but, for the 24-elements, these pads are located on both sides of the array. Two test elements are also provided for checking array processes.

The main problem in any two-dimensional array structure is to obtain a complete transfer of charge between the row and column gates in each resolution element. Figure 3 illustrates the situation. Each resolution element consists of two separate storage gates, coupled so that charge can be readily transferred between the two storage sites. During the charge-storage period, photon-generated charge is stored in both the row and column gates at each sensing site. When the vertical scan register selects a row line, the signal charge at every gate in that line is transferred to the corresponding column gates by setting its voltage to zero (shown as a row-select in Figure 3). Then, the charge at the selected site is injected by applying an injection pulse through a selected column line; but, at the same time, any charge in the unselected elements of that column must be transferred into the corresponding row gates to avoid injection (shown as a non-row select in Figure 3). Therefore, charge injection and transfer must occur on the basis of element selection. For selected elements, the charge is injected to yield a signal, while for unselected elements, charge must be transferred to avoid injection. The result is sequential readout.

Charge-coupling between gates in each resolution element is accomplished by an overlapped gate structure. Three different structures with overlapped gate configurations were investigated.

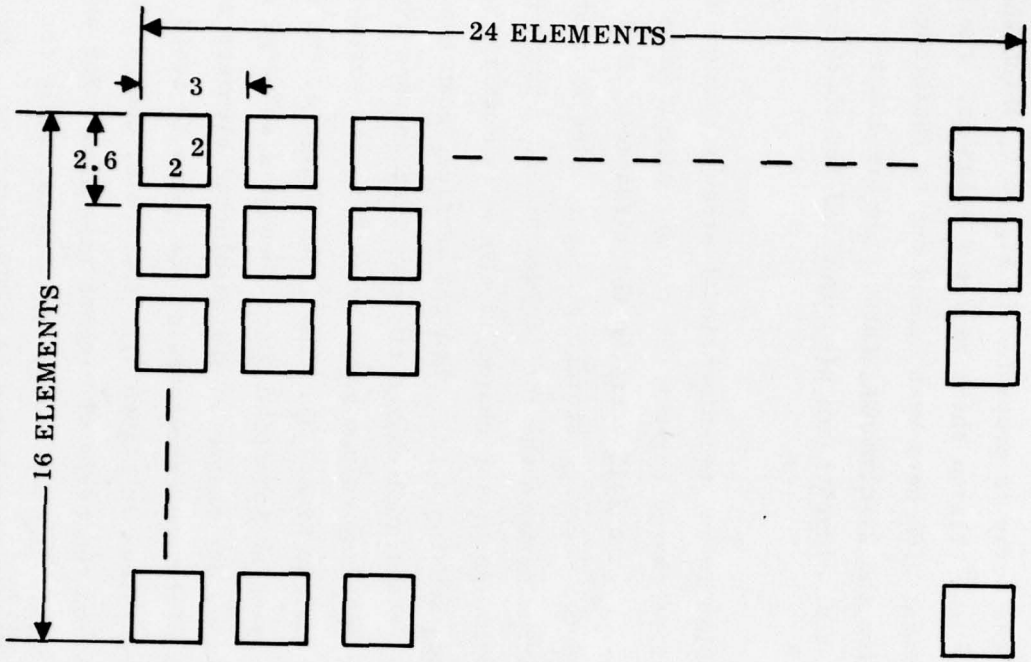


Figure 1. Layout of Resolution Elements for 16x24 InSb CID Array, Showing All the Dimensions.

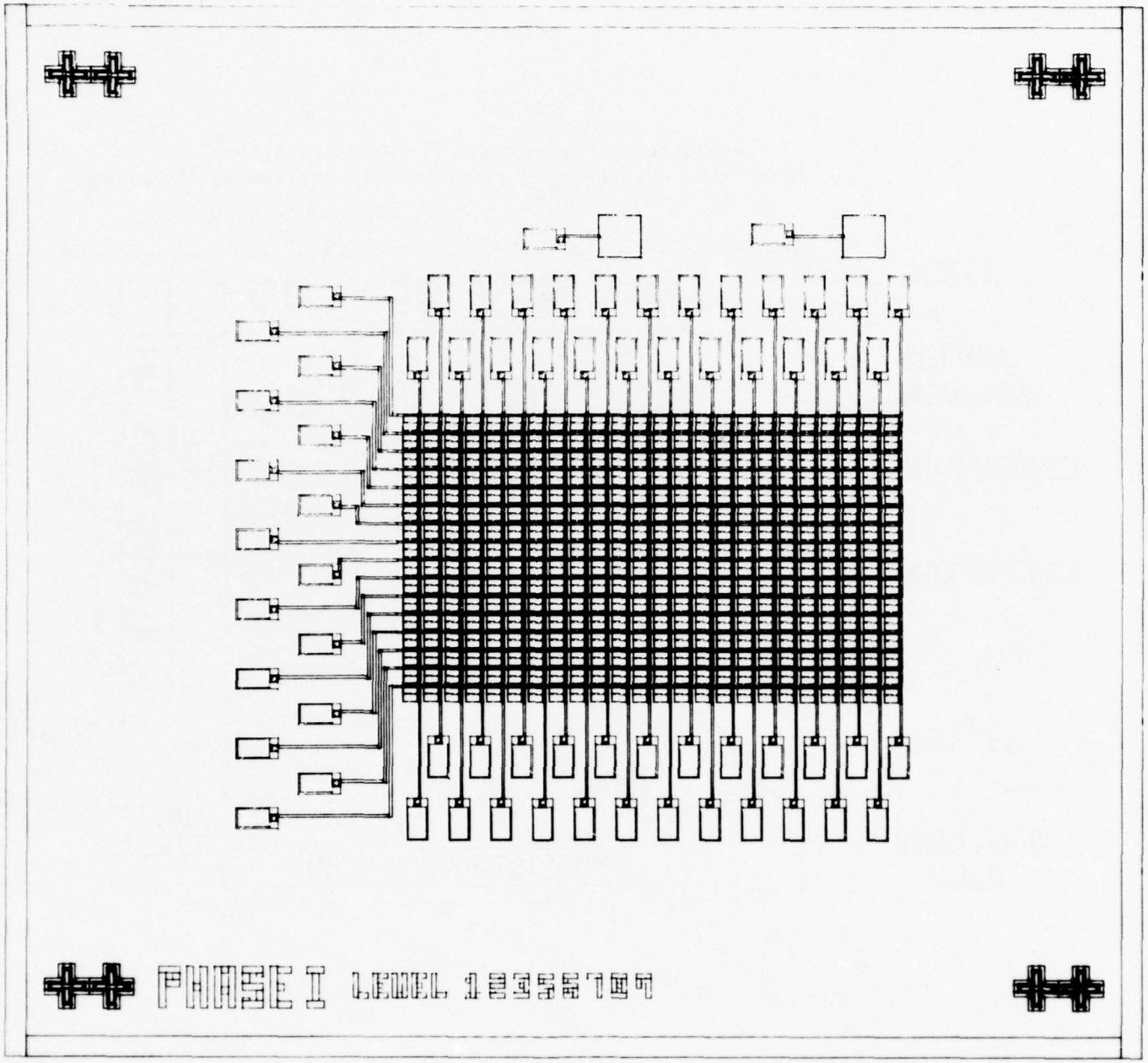


Figure 2. Complete Layout of 16x24 Array Mask Patterns Showing the Bonding Pads for Silicon Shift Register Scanner Interconnection.

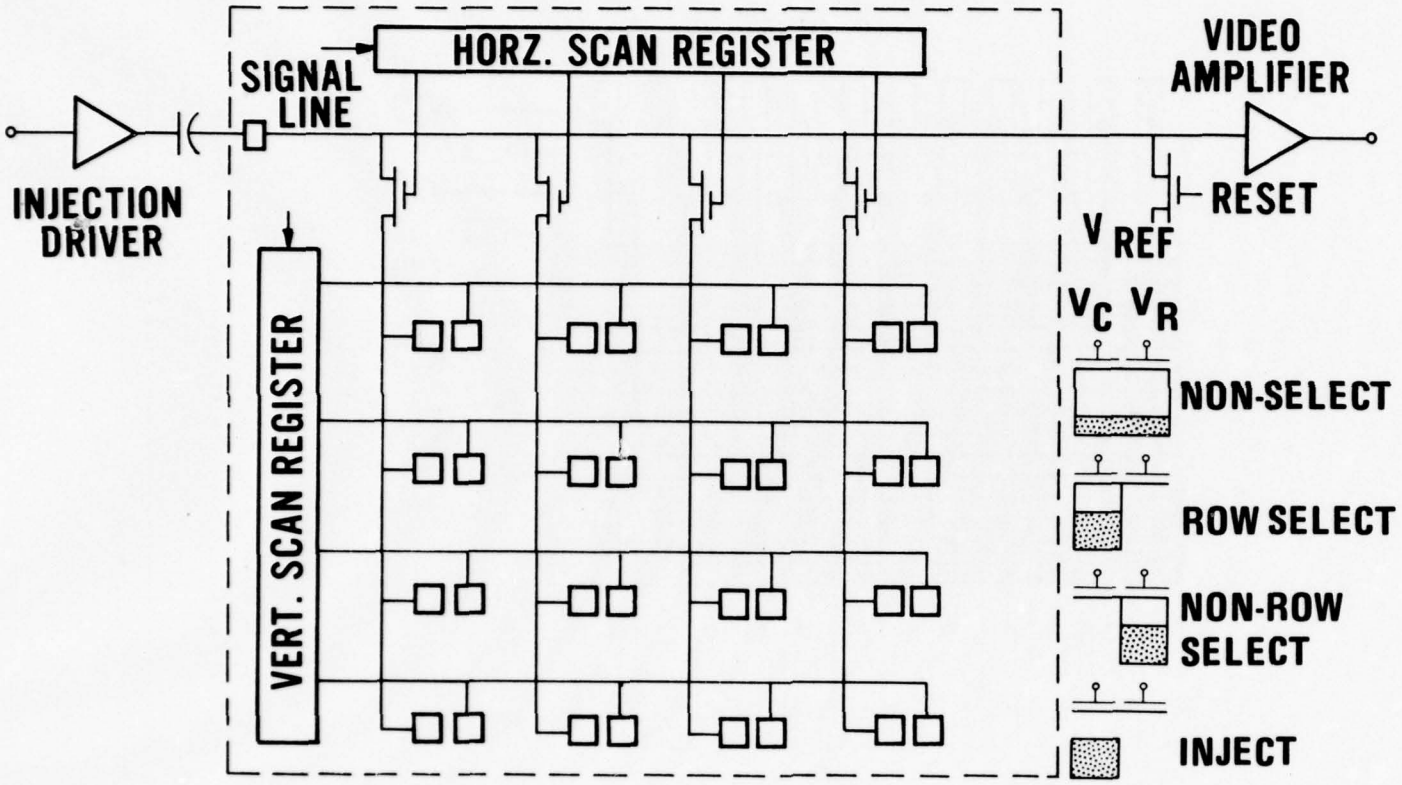


Figure 3. Sequential Readout for CID Two-Dimensional Array, Requiring Proper Charge Transfer Operation.

1. One-side Overlapping with Parallel Gates

The unit cell of this array structure, including a cross-section of the active region, is shown in Figure 4. The oxide thickness between the two gates is, typically, 1000Å, and the oxide thickness of the top gate is roughly twice that of the bottom gate. This type of structure has an inherent problem. That is, for deep potential wells, the gate oxide thickness should be as thin as possible, which, then, becomes a very thin oxide layer between the gates. This thin overlayer, in turn, causes an increased capacitive coupling between the two gates and, thus, a large pattern noise in the output video signal. A structure that alleviates this situation involves coplanar gates.

2. One-side Overlapping with Co-planar Gates

This structure is similar to the above described configuration except that the two gates are located co-planar to each other. Here, since both row and column gates are located on, roughly, the same thin oxide, deep potential wells can be created and charge transfer is readily accomplished. The step oxide thickness between the two gates is approximately 1000Å, which is sufficiently thick to minimize any capacitive coupling between the row and column gates in each resolution element. This thick step oxide also reduces the possibility of shorting between the two gates and, thus, processing yields are increased. Also, with this configuration, the array performance has been much improved. With this configuration, however, there may be a problem in the row and column crossover regions, in that the final array may be so thick that the oxide may crack due to strain. The following structure has been prepared to solve this problem.

3. Multi-sides Overlapping Arrays

The unit cell of this structure involves multi-side overlapping, which increases the probability of charge transfer.[2] Also, the crossover region of the row and column bus lines has been located on the active gate area in a manner that minimizes the overall thickness of the crossover areas. The unit cell structure is shown in Figure 5. Three y-sides have been overlapped and the x and y crossover regions are located at the center of

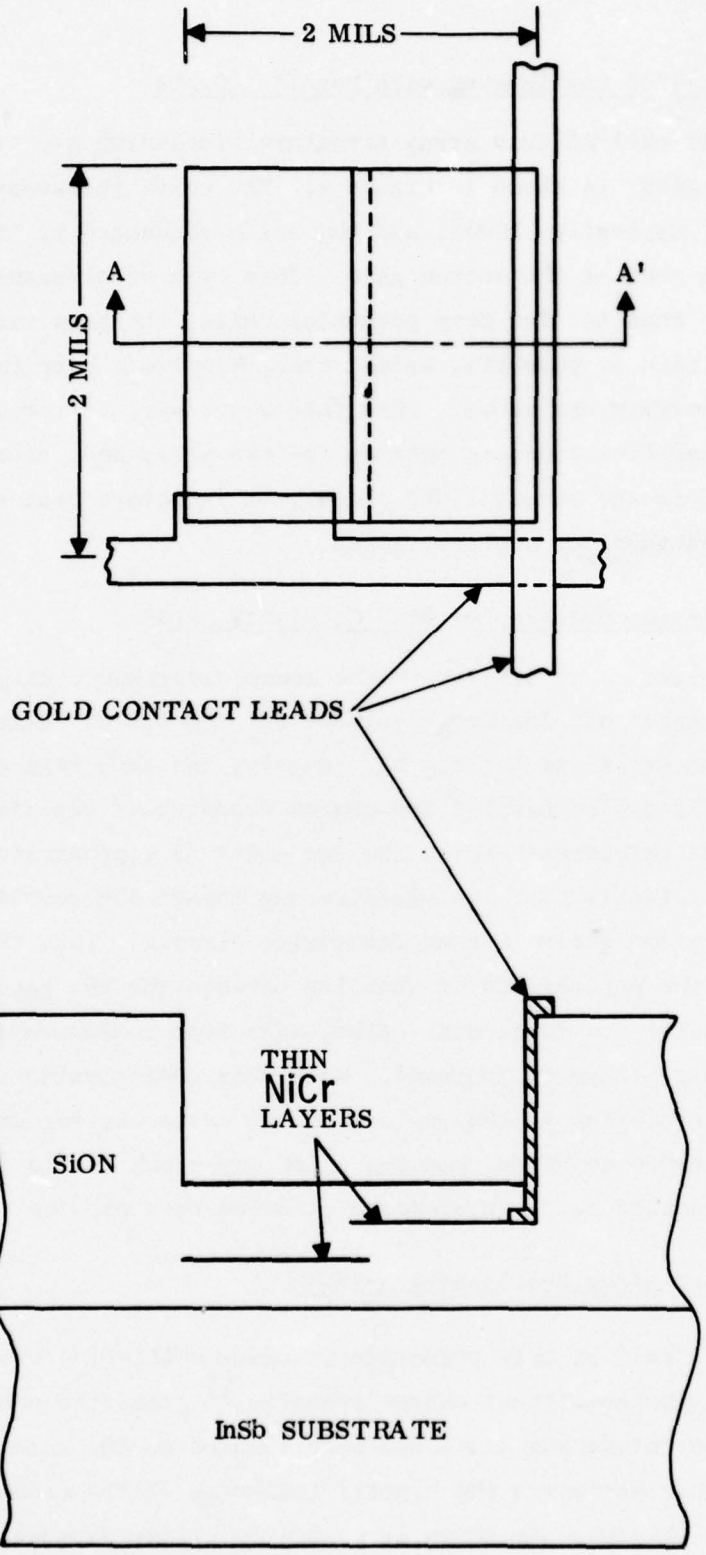


Figure 4. Resolution Element of Array Structure for One-Side Overlapping with Parallel Gates.

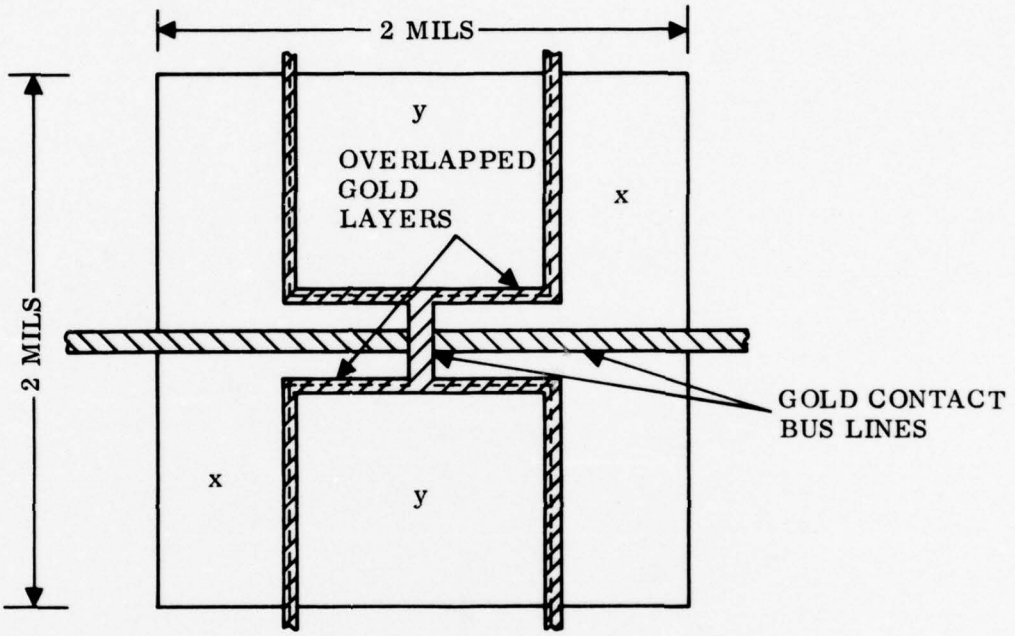


Figure 5. Resolution Element for Multi-Sides Overlapping Array Structure.

the active gate areas. The gold contact bus lines that cross the center area and connect all of the gates are high conductivity metal layers. One disadvantage of this configuration is that the area of the optical collecting sites are reduced because of the additional gold layers, which are opaque.

SECTION III. ARRAY FABRICATION

1. Introduction

The InSb CID array processing technology developed on the previous program[1] culminated in a 1x16 single-column two-dimensional structure. This technology has now been extended to two-dimensional 16x24 area arrays. Now, however, because of the increased array area and the many multilevel crossovers, the processing procedures had to be changed considerably to cope with the following problems:

a) non-uniform metallized step coverage at thin-thick oxide regions and x-y crossovers, which result in open interconnections

b) particle inclusions, which increase defects in the active areas

c) poor adherence in the structures, leading to reduced bond reliability.

As pointed out in Section II, charge transfer between row and column gates in each resolution element of the two-dimensional structure is a major problem in the development of area arrays. To operate properly, charge transfer and injection must occur according to element selection. The charge injection is readily accomplished, but charge transfer is not so easy, depending on many array processing functions. We selected an overlapped-gate type of structure between the row and column gates in each resolution element to obtain charge transfer. The configuration was fabricated via a multilevel metallization process, in conjunction with SiON oxide layers which served as the gate and field oxides and as insulators for isolation between metallic layers.

We investigated the following three different array structures (as discussed in Section II):

1. One-side overlapping with parallel gates, Phase I - 16x24.
2. One-side overlapping with co-planar gates, Phase I-Modified 16x24.
3. Multi-sides overlapping array structure, IRA2 - 16x24.

The array processing steps for each of these structures are quite similar and, therefore, we will discuss the fabrication of only one of them, namely the Phase I - 16x24 array, which has received the major share of the effort.

2. Array Fabrication Processes

A) Material Preparation

N-type InSb single crystals, doped in the range of 10^{14} to 10^{15} cm^{-3} were employed. These materials have a low etch-pit dislocation density, less than 100 EPD/cm^2; all were purchased from outside vendors in the form of ingots. The ingots were sliced into wafers and polished to a mirror-like surface. The polished wafers were then polished further in a lactic-nitric acid solution. The wafers were coated with a SiON dielectric layer.[8] For this initial deposition, a relatively thick oxide coating (approximately 5000Å) was used.

B) Wafer Inspection

The oxide-coated wafers were inspected for particle inclusions, defects and uniformity prior to the first oxide cutdown process. Sample wafers from each deposition were also tested for initial oxide/substrate interface adherence and the C-V characteristics were measured.

C) Resolution Elements Formation

After inspection, the wafers were coated with a Kodak negative resist, precured in nitrogen, exposed, developed and spun dry. They were then post-curec in nitrogen. The thin gate resolution element areas were controlled to a thickness of about 1400Å. The thickness of these gates was determined approximately by checking against a color chart. The photoresist was removed with micro-stripper and the wafers were rinsed in cascaded water and blown dry. The scribe line on the oxide mask was also used to measure the thickness of the gate oxide more precisely, after photoresist removal. Figure 6 shows the resolution element geometry.

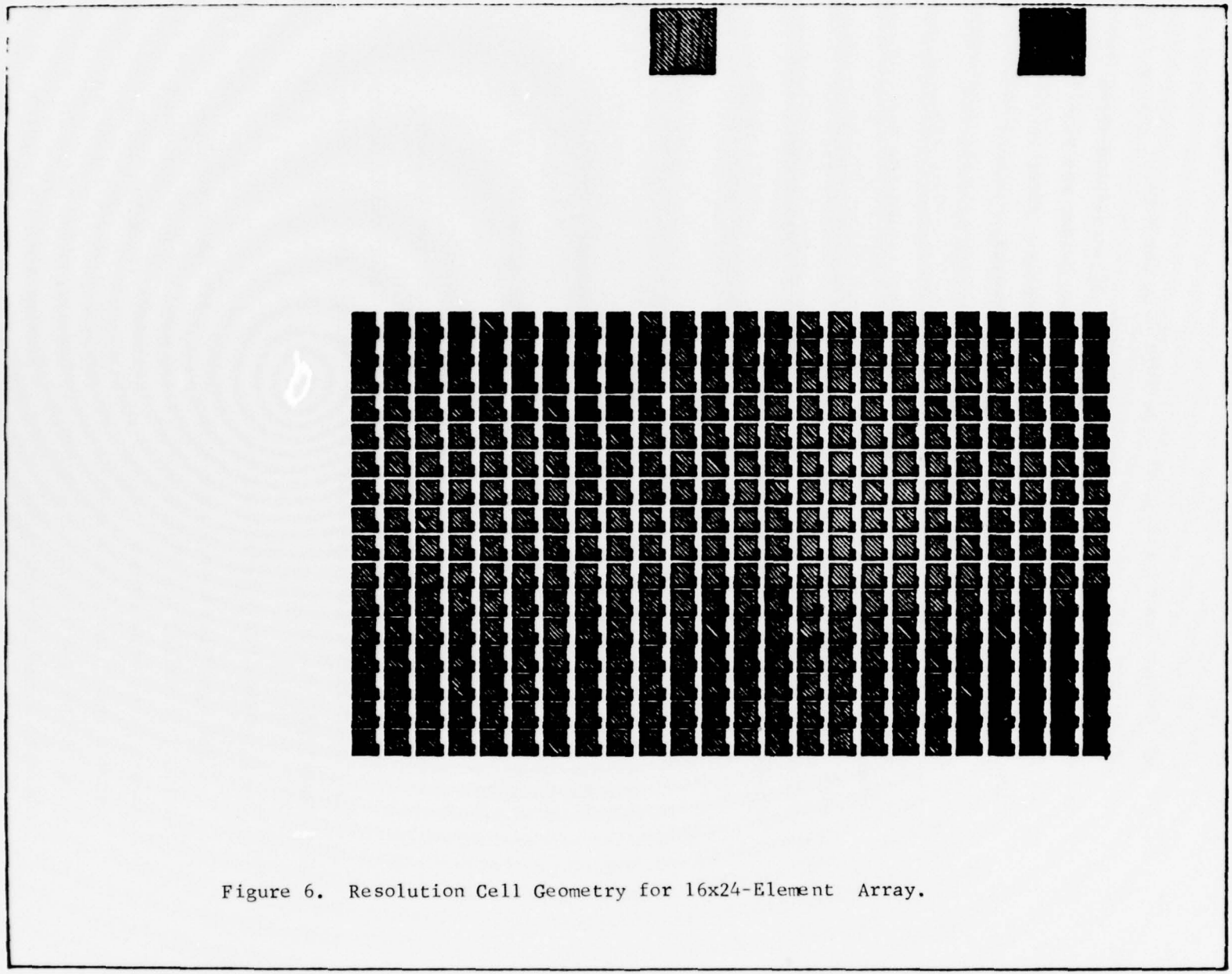


Figure 6. Resolution Cell Geometry for 16x24-Element Array.

D) Vacuum Deposition of NiCr-Au Thin Film for X Metal Layers

The wafers were loaded into a Veeco 775 vacuum station which was evacuated to about 5×10^{-7} torr. The wafer holder was heated and the NiCr and gold were deposited sequentially. After metallization, the wafers were cooled in vacuum and removed.

E) Patterning of X Sensor Gates and Lead Interconnections

The wafers were again photoresist patterned, using the mask shown in Figure 7. After removal of the photoresist, the wafers were inspected to determine the resolution of the array geometry. Note that the linewidths are 0.3 mils. The C-V characteristics of the MIS test devices, which are equivalent to the X sensor gates, are checked after this processing step.

F) Formation of X Sensor Gates

The wafers were again coated with resist, precured, exposed, developed and post-cured. The transparent X sensor gates were formed by removing the gold using the mask shown in Figure 8. The wafers were then quenched, the photoresist was stripped, and the wafers were cleaned and dried.

G) Oxide Deposition for Gate and X-Y Cross over Isolation

After the wafers were rinsed in cascaded water and blown dry, they were loaded into the oxide reactor and the isolation oxide was deposited.

H) Oxide for Y Sensor Gates

Once again the wafers were spin-coated with Kodak negative resist, precured, exposed, developed and post-cured. Then the Y sensor gates were formed, leaving about 1000Å isolation oxide between the X and Y gate region. The thickness of the isolation oxide at the X-Y crossover regions is, however, about 3000Å to minimize capacitive coupling. This processing step was carried

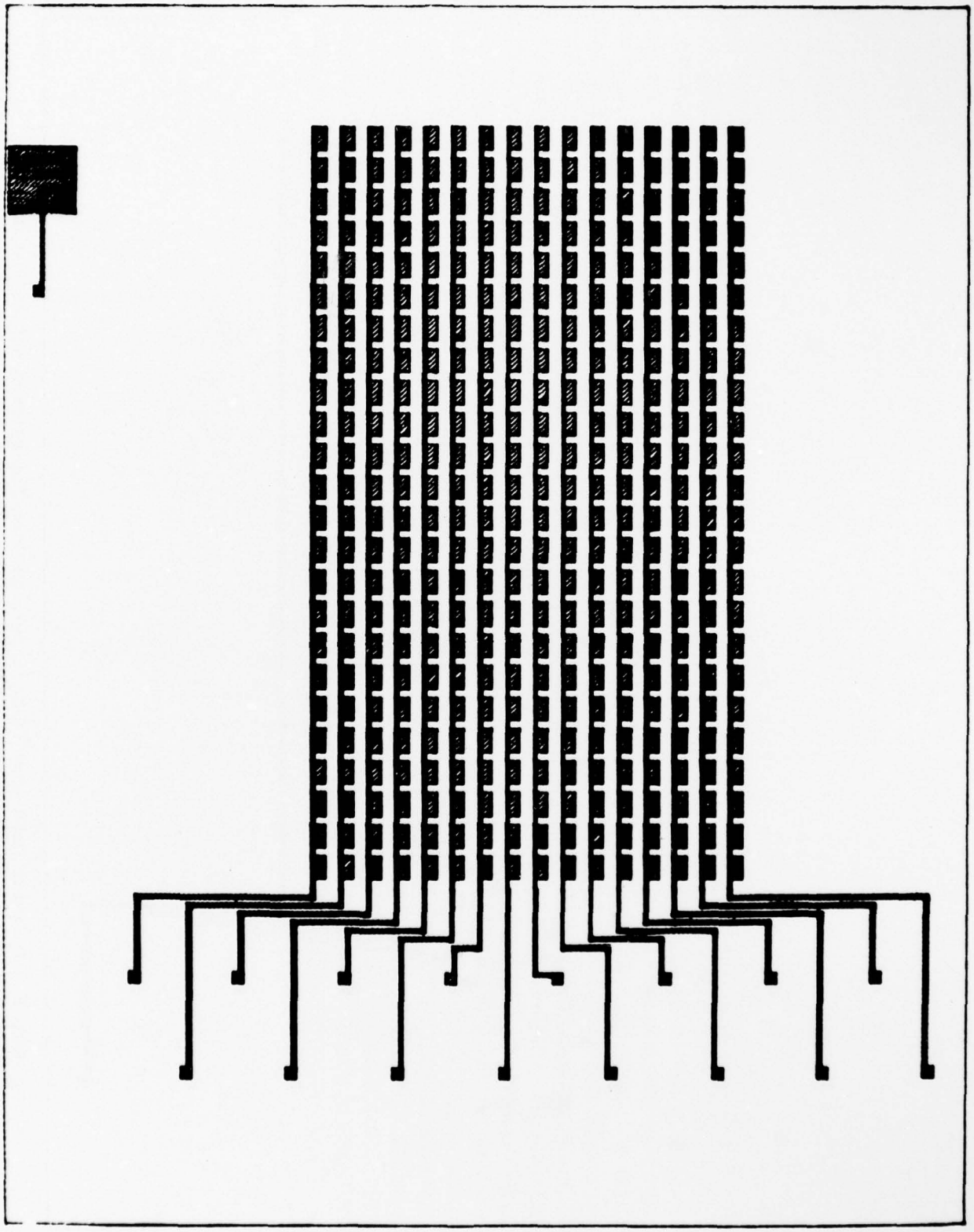


Figure 7. NiCr-Au Pattern for X Sensor Gates (Rows) and Leads.

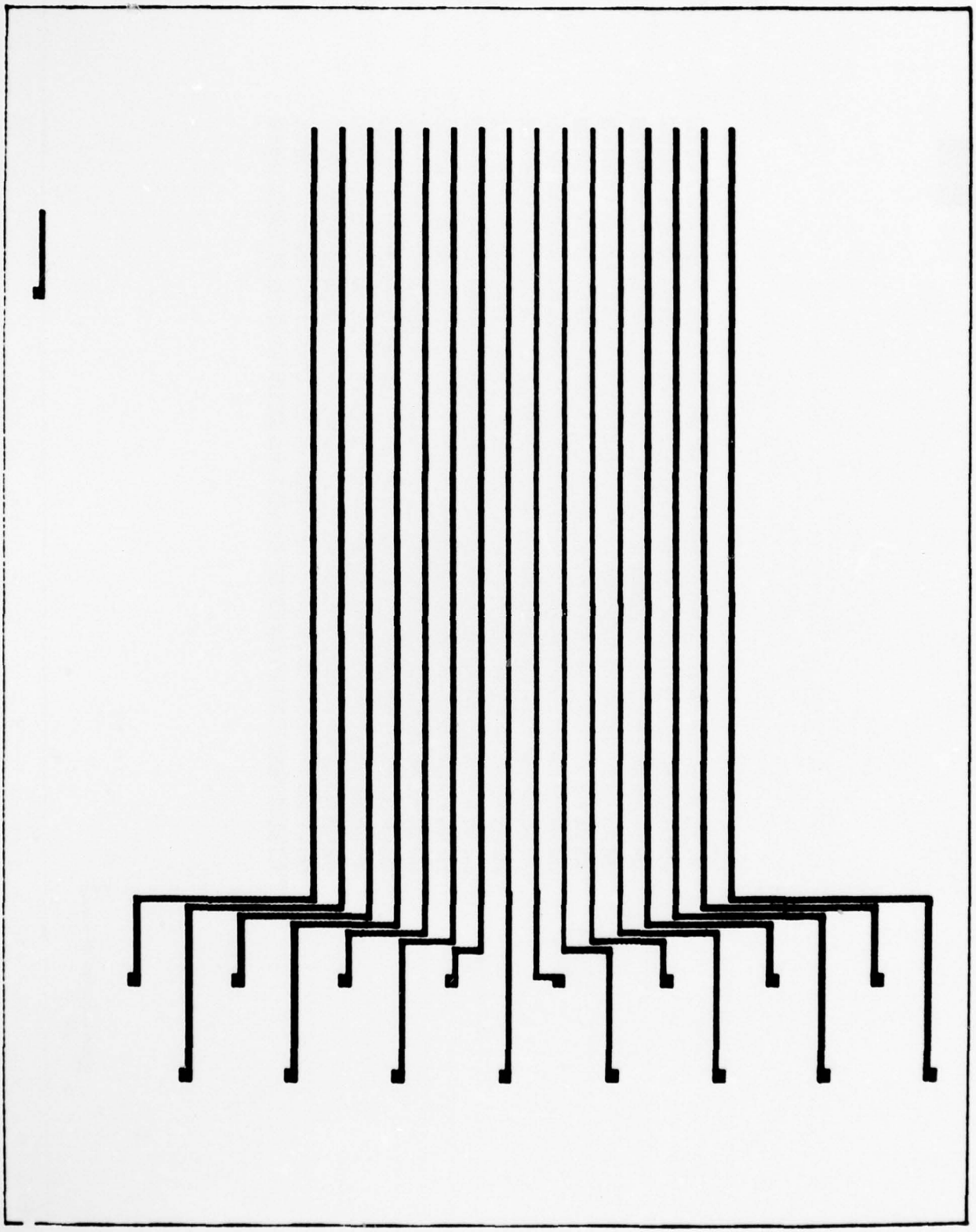


Figure 8. X Sensor Gate Lead Pattern Used to Form Transparent Active Row Cells.

out using the mask pattern shown in Figure 6. The photoresist was then stripped and the wafers were thoroughly rinsed and dried. The C-V characteristics of the device were then checked.

I) NiCr-Au Thin Film Deposition for Y Metal Layer

The wafers were loaded into the rotating flat plate substrate holders, and the system was evacuated to 5×10^{-7} torr. To promote adherence of the thin films the wafer holders were heated. After the thin films were deposited, the wafers were cooled in the evaporator.

J) Patterning of Y Sensor Gates and Lead Interconnections

Photoresist was again applied to pattern the Y sensor gates and leads, using the mask shown in Figure 9 . The unmasked photoresist areas were etched, sequentially, to remove both metal layers. Then, the wafers were rinsed in deionized water, blown dry and placed in the microstrip to remove the photoresist. They were then thoroughly cleaned in the cascading water bath.

K) Formation of Y Sensor Gates

Kodak negative resist was applied, precured, exposed, developed and post-cured. The wafers were then loaded in the wafer holders to form the transparent Y-sensor electrodes by removing the gold layer. The array patterns were then inspected for edge definition and imperfections. The mask pattern for this step is shown in Figure 10.

L) Oxide Deposition for Surface Protection

The final oxide layer is deposited in this step. The glass acts as a passivation layer, protecting against abrasion of the array elements, and against moisture and the ambient.

M) Contact Window Etching

The contact windows for the bond pads were etched using a photoresist process, as before. This step removes the two previously deposited oxide coatings. Figure 11 shows the mask pattern used. After cleaning the photoresist, the wafers are ready for the final metallization step.

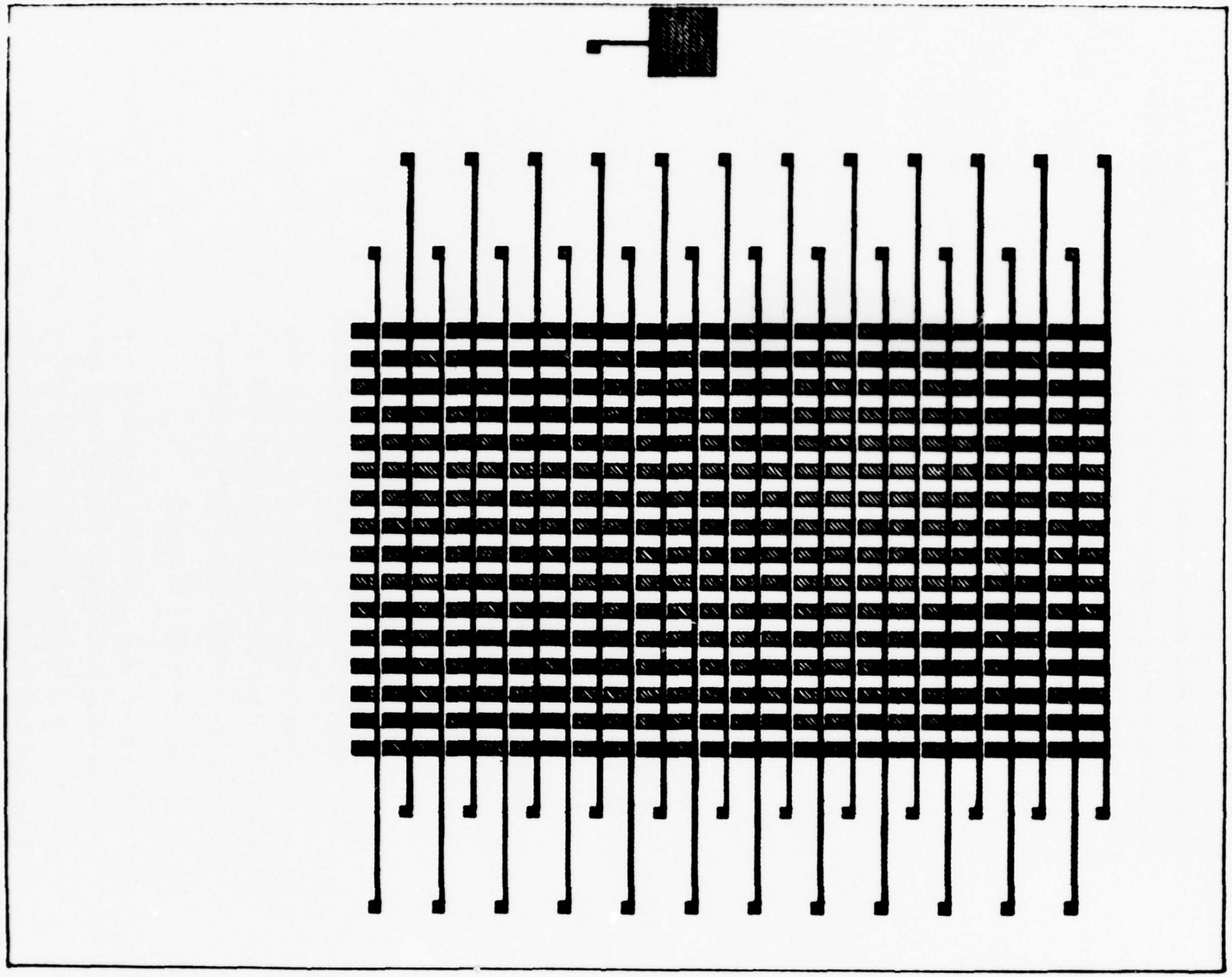


Figure 9. NiCr-Au Pattern for Y Sensor Gates (Columns) and Leads.

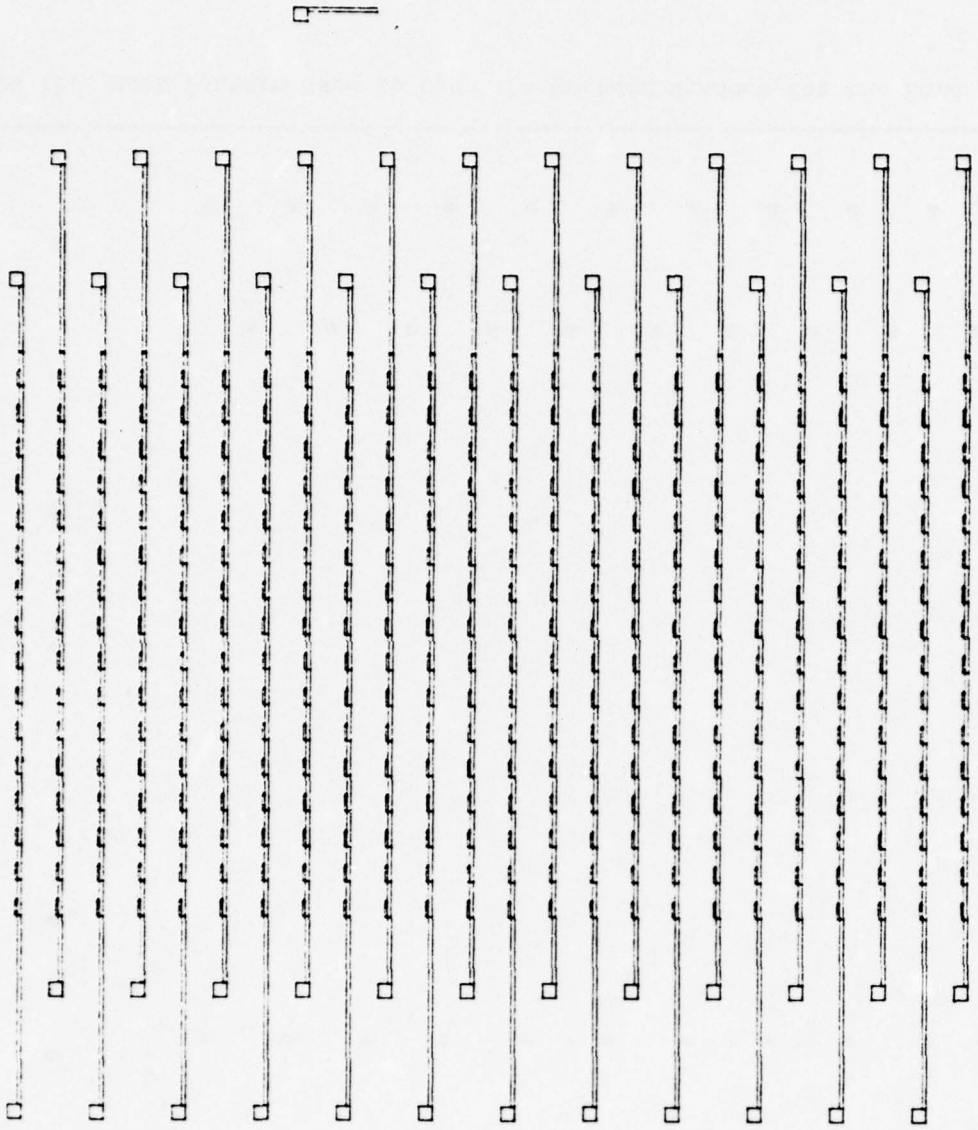


Figure 10. Y Sensor Gate Lead Pattern Used to Form the Transparent Active Column Cells.

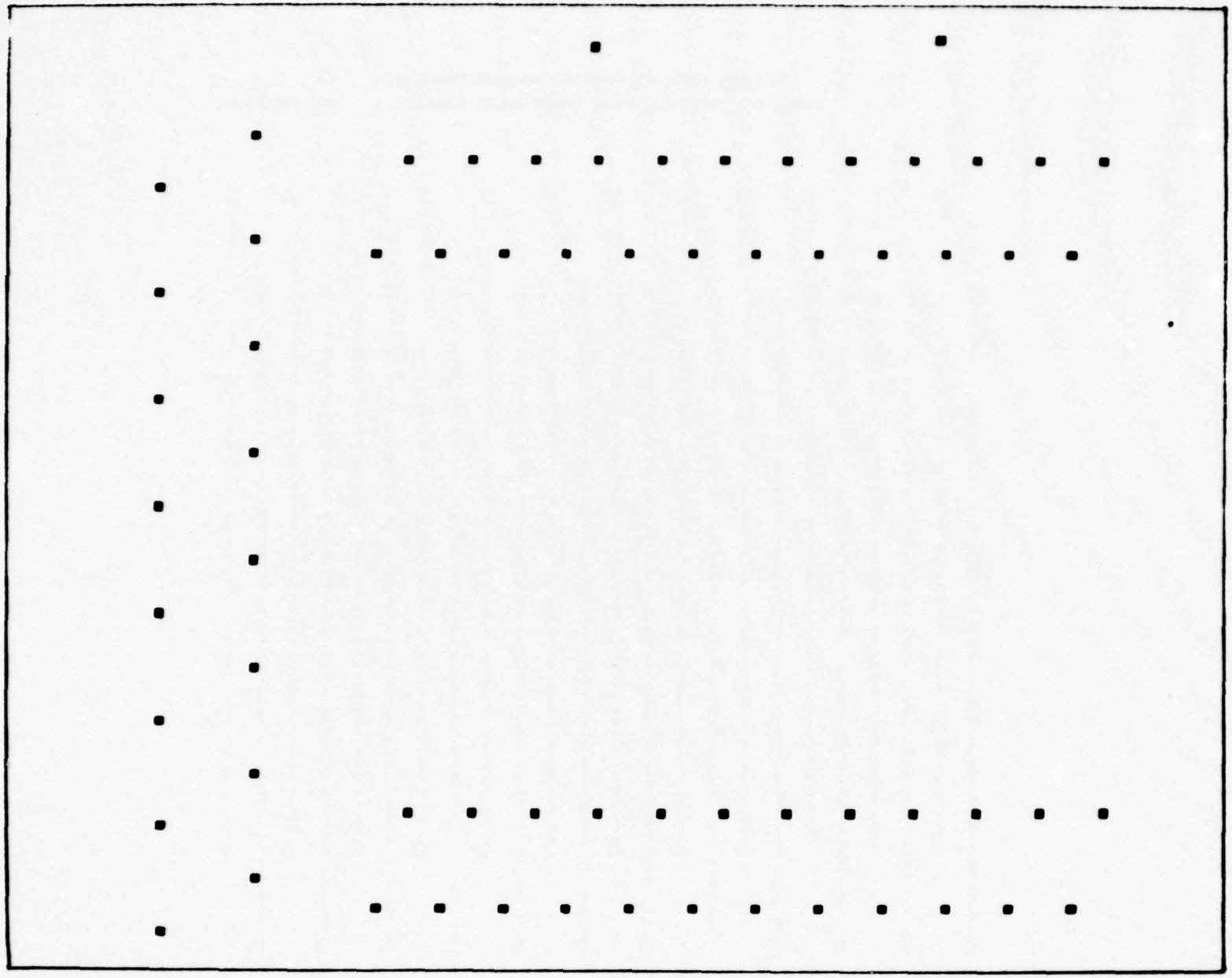


Figure 11. Mask Pattern Used to Open the Contact Windows for the Bond Pads.

N) Thin Film Deposition of Ti-Au for Bonding Pads

In our earlier work, we employed Cr-Au on NiCr-Au for bonding pads. Later, we switched to Ti-Au bonding pads and found that adherence was significantly improved. The wafers were loaded in the vacuum system, evacuated to 5×10^{-7} torr and heated. A standard spiral charged with titanium wire was used to deposit Ti; gold was deposited from a tungsten dimple boat.

O) Delineation of Bonding Pads

The wafers were coated with photoresist, the gold was etched away and then the Ti metal layer was removed. The mask pattern used for this processing step is shown in Figure 12. After the bonding pads were delineated, the wafers were given a final cleaning and thorough inspection.

The following inspection procedures were used:

1) All wafers were microscopically inspected for open runs, dirt-defect inclusions and substrate surface damage due to handling.
2) The sensor arrays were checked for C-V characteristics. First, the arrays were probed at $300^{\circ}K$ for the room temperature oxide capacitance; then they were scribed and evaluated at $77^{\circ}K$, using standard C-V data.
3) Selected arrays were packaged to evaluate array operation.

Figure 13 is a photomicrograph of a typical, completely processed 16x24 InSb CID array. A typical final array wafer, containing many array chips, is shown in Figure 14. For low temperature C-V measurements, we mounted the final array chip on a flat-pack package and connected several row and column lines. Figure 15 shows typical C-V data for four rows and five columns of an array, one-side overlapping with parallel gates. Note that the transitions occur at about the same gate voltage for row and column lines, respectively, indicating that the C-V characteristics are uniform. The high flat-band voltage observed for the row lines is attributed to a thick row gate oxide, which is one of the problems encountered in this structure.

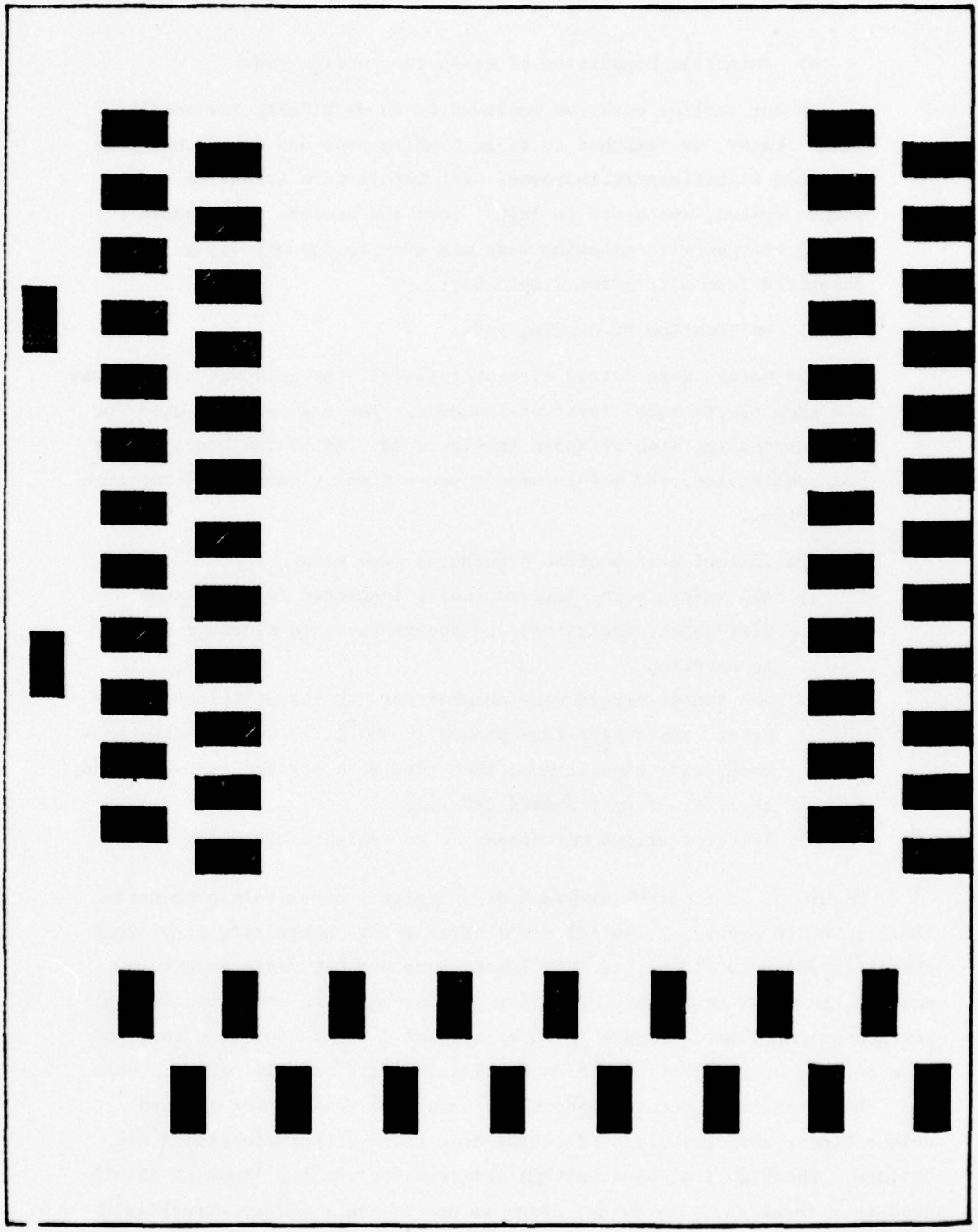


Figure 12. Mask Pattern for Bonding Pads.

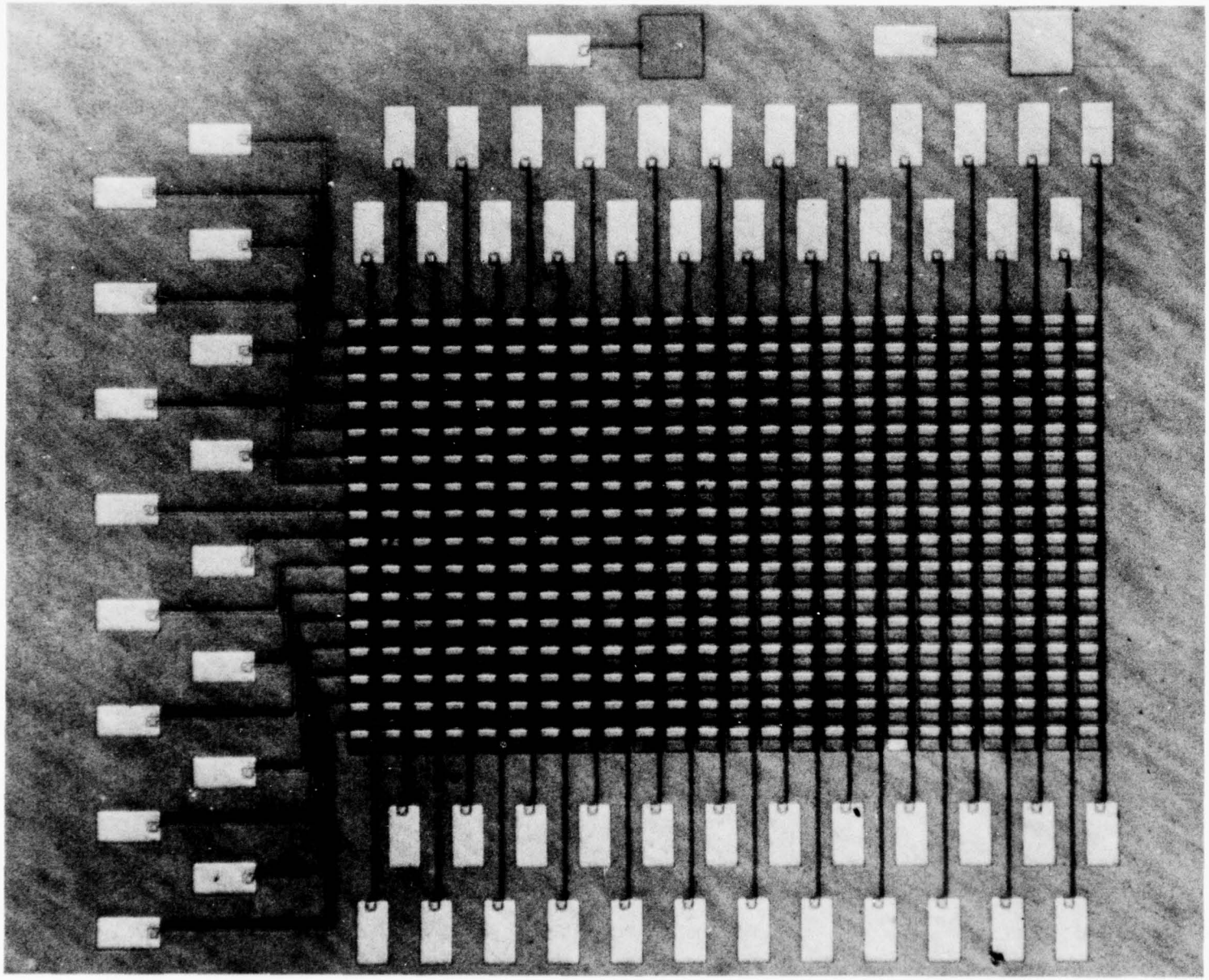


Figure 13. Photomicrograph of Completely Processed 16x24 InSb CID Array. (One-Side Overlapping with Parallel Gates).

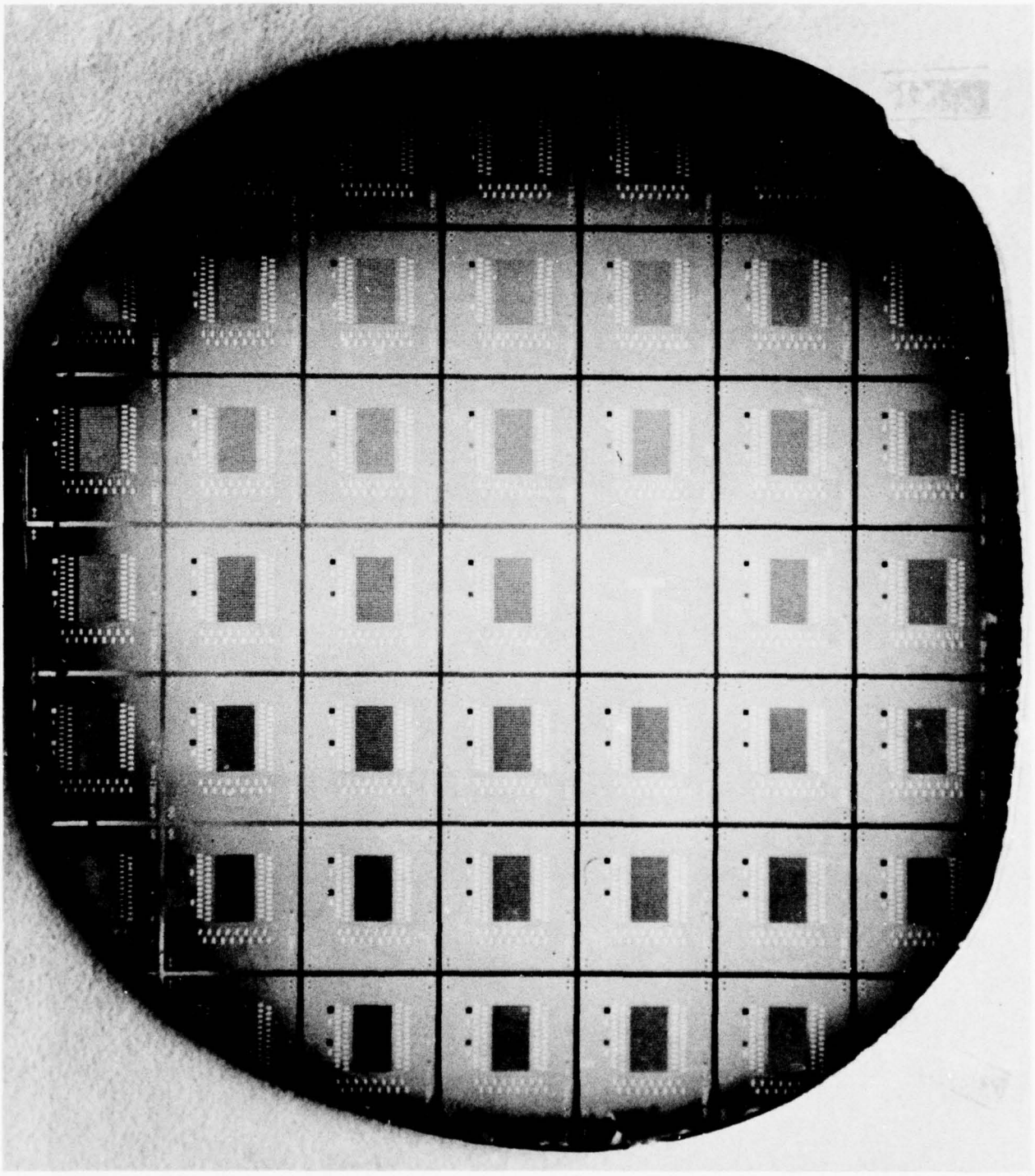


Figure 14. Photograph of a Typical Final Array Wafer, Containing Many Array Chips.

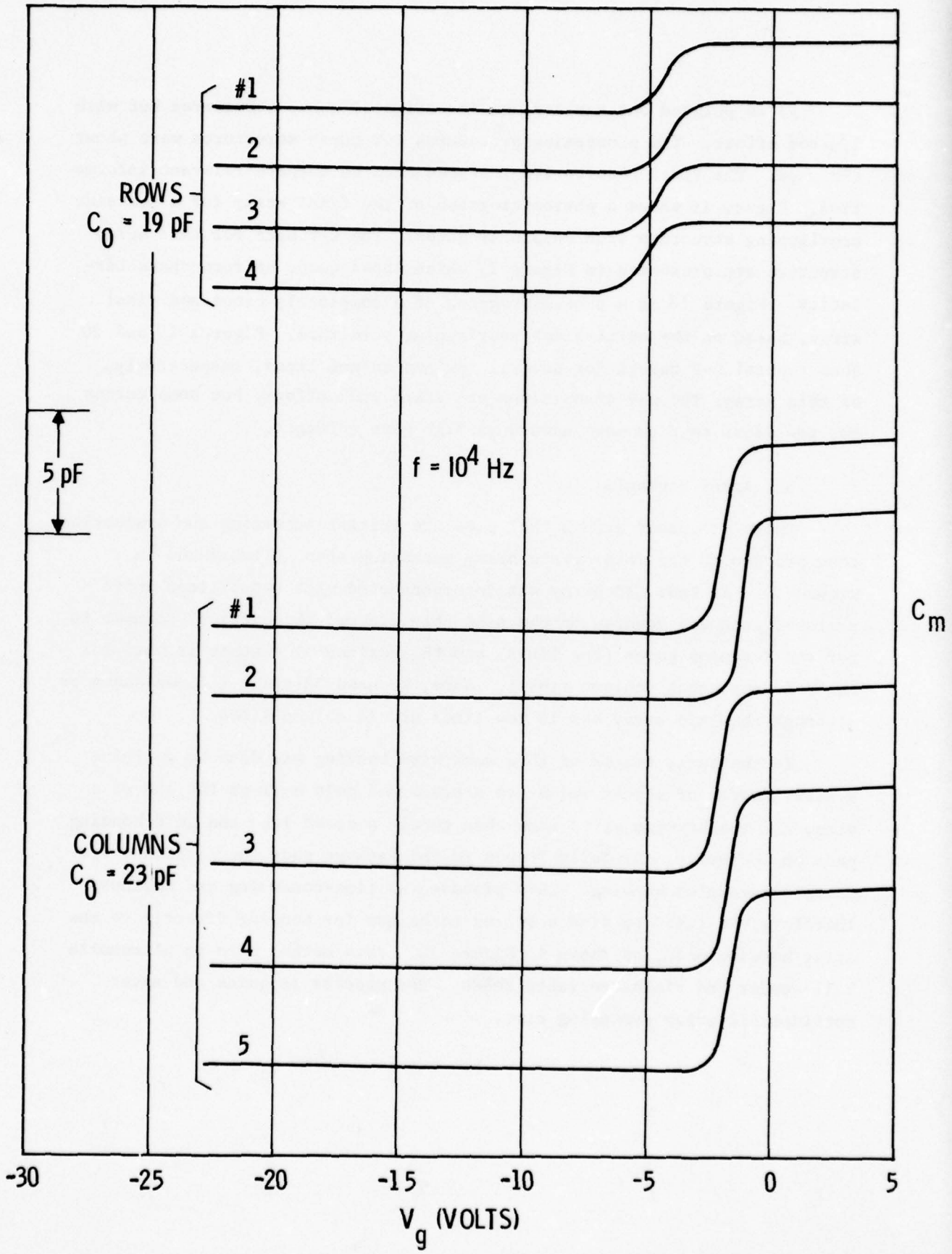


Figure 15. C-V Characteristics for the Array Structure of One-Side Overlapping with Parallel Gates.

As we pointed out earlier, we investigated other structures but with limited effort. The processing procedures for these structures were about the same. The final results are reported here to compare relevant information. Figure 16 shows a photomicrograph of the final array for a one-side overlapping structure with co-planar gates. The C-V data for this array structure are presented in Figure 17 which shows good, uniform characteristics. Figure 18 is a photomicrograph of a completely processed final array, based on the multi-sides overlapping structure. Figures 19 and 20 show typical C-V curves for several row and column lines, respectively, of this array. The C-V transitions are sharp and uniform, but some curves for row lines tend to move upward at high gate voltages.

3. Array Packaging

Those processed arrays that pass the initial screening and evaluation, then proceed to the focal plane array packaging step, illustrated in Figure 21. An InSb CID array was interconnected with two silicon shift register scanners mounted on the same cold finger; the vertical scanner is for the X-sensor gates (row lines) and the horizontal scanner is used for the Y-sensor gates (column lines). Here, we used 32-stage silicon scanners, although the InSb array has 16 row lines and 24 column lines.

In the early stages of this work,wire bonding was done by applying a small amount of molten indium to a preformed gold ball at the end of a wire, and the bonding wires were then gently pressed into the gold bonding pads on the array, carefully looped to the package pads, and attached via thermocompression bonding. This process was time-consuming and tedious. Therefore, we tried to find a better technique for bonding directly to the array bonding pads, as shown in Figure 18. This method uses an ultrasonic ball-bonder and yields reliable bonds. The process is quick and saves considerable array packaging time.

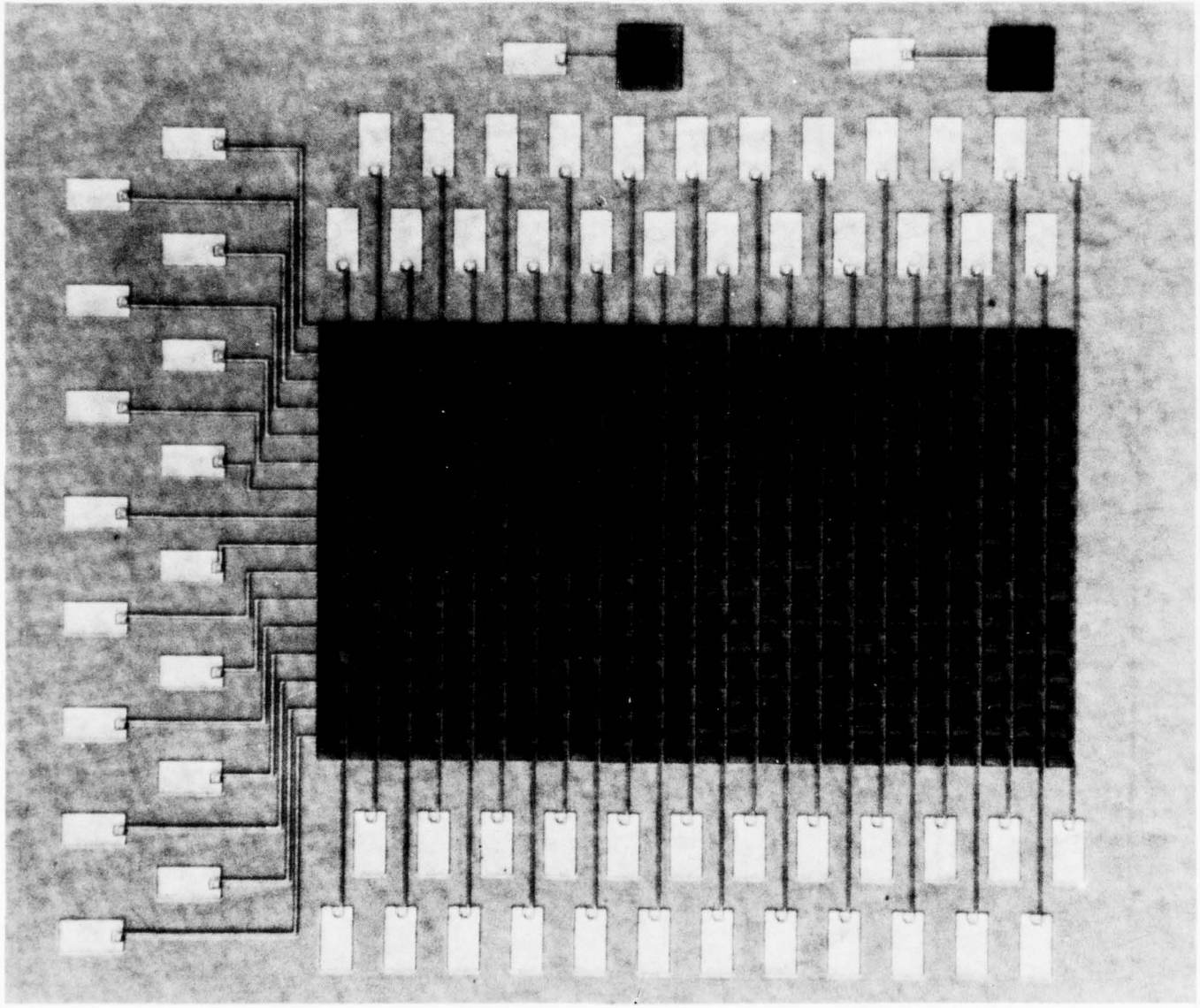


Figure 16. Photomicrograph of the Final Array for One-Side Overlapping with Co-Planar Gates.

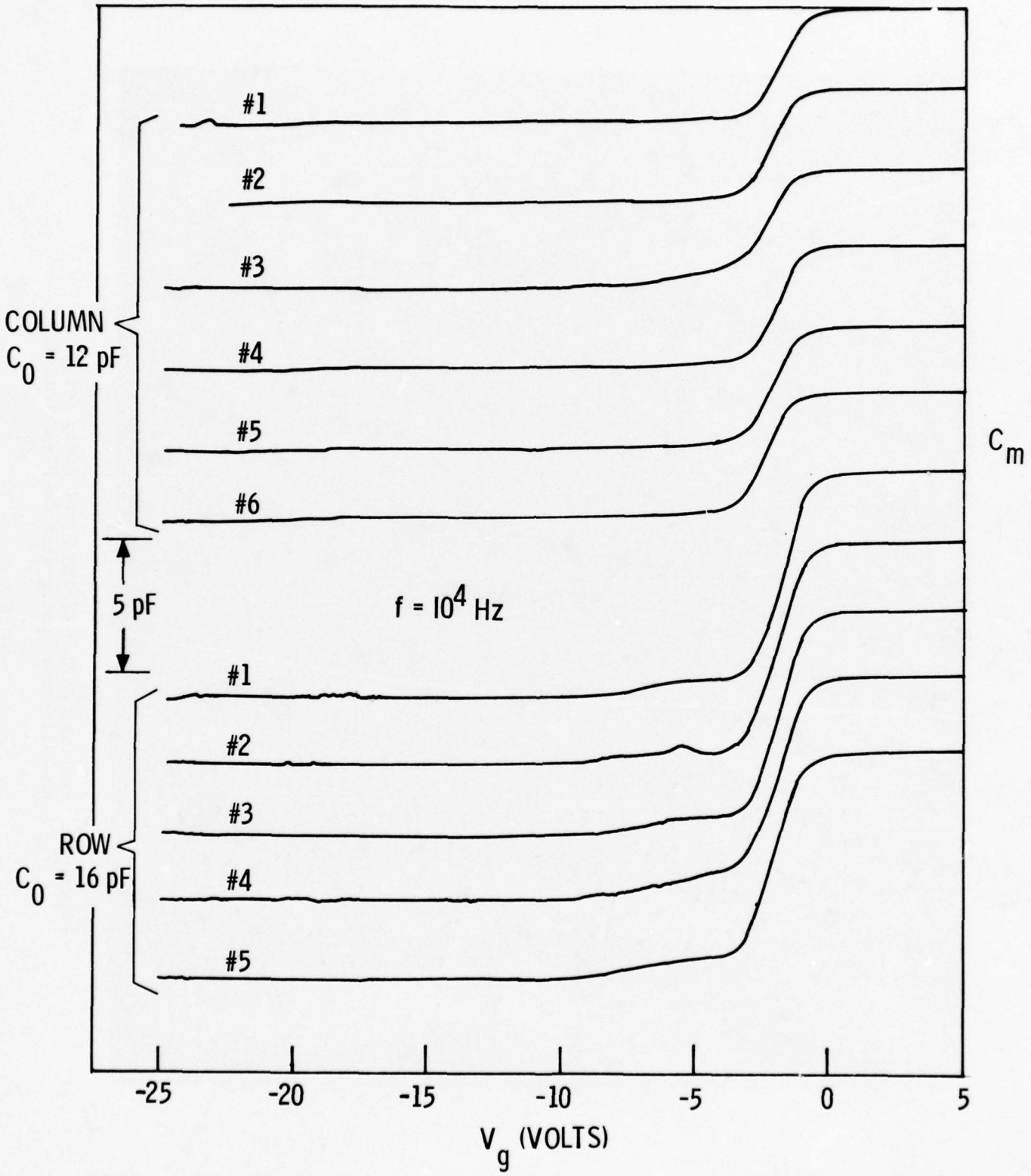


Figure 17. C-V Characteristics for the Array Structure of One-Side Overlapping with Co-Planar Gates.

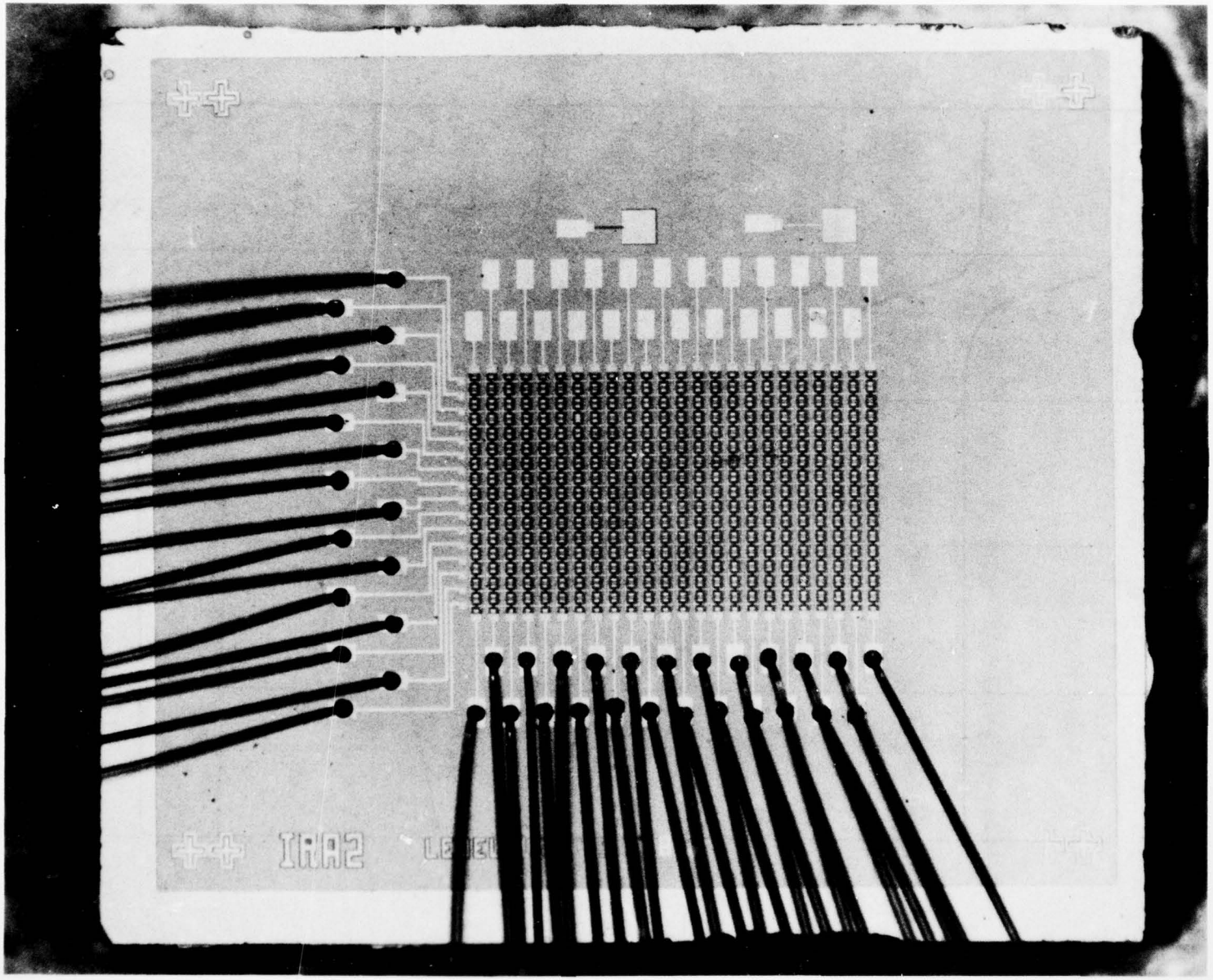


Figure 18. Photomicrograph of Completely Processed Final Array, Based on the Multi-Sides Overlapping Array Structure.

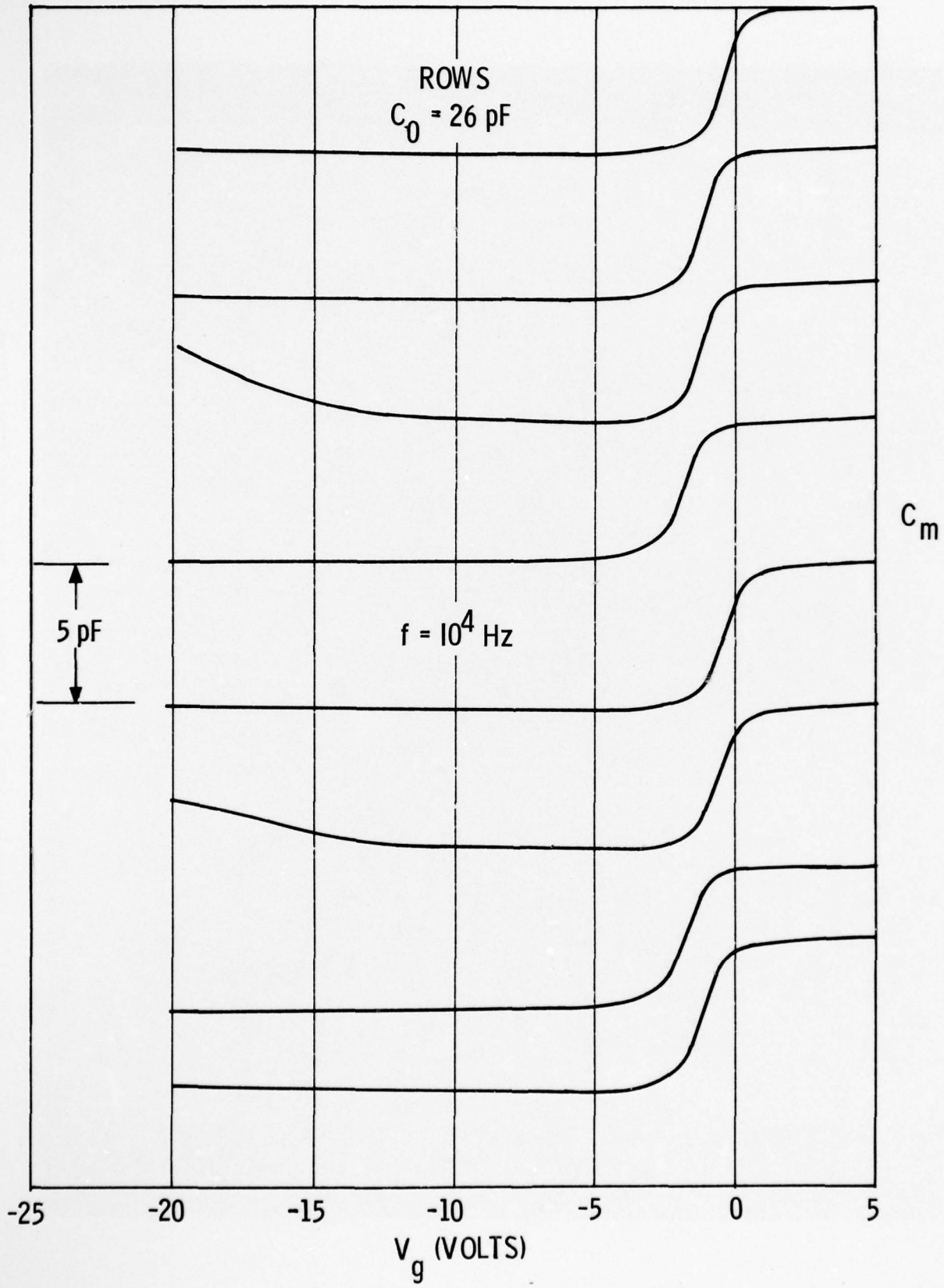


Figure 19. C-V Characteristics for Several Row Lines of Multi-Sides Overlapping Array Structure.

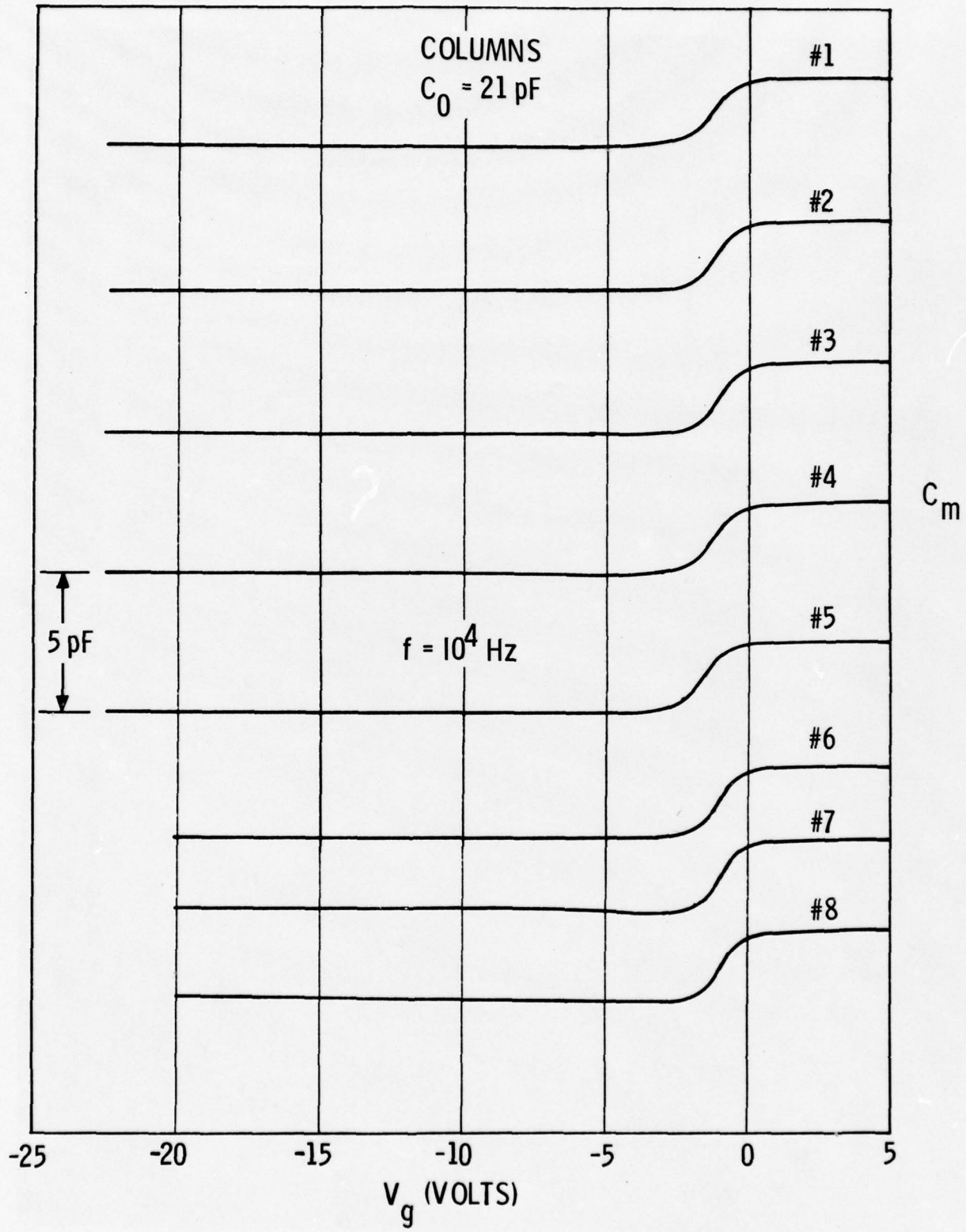


Figure 20. C-V Characteristics for Several Column Lines of Multi-Sides Overlapping Array Structure.

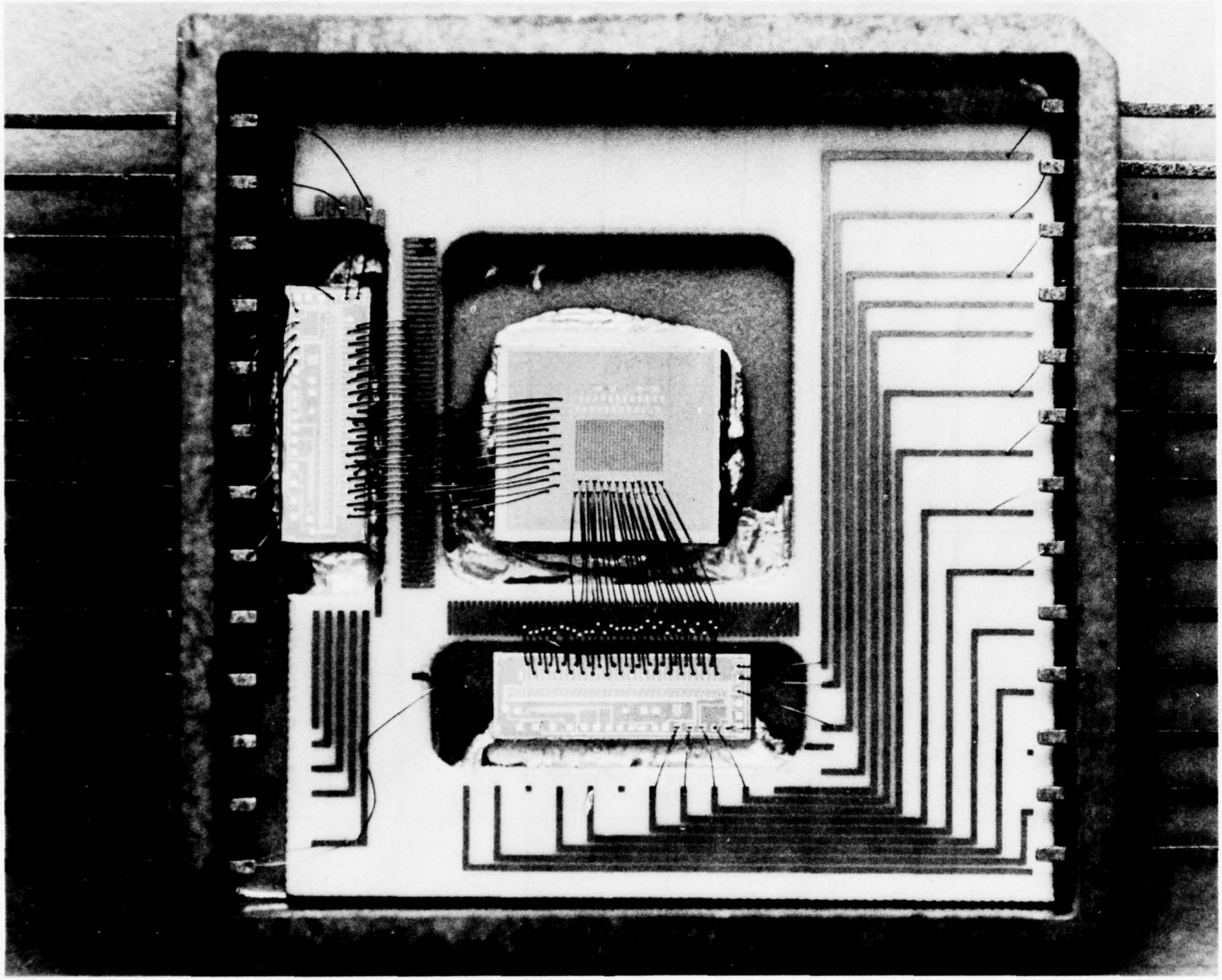


Figure 21. Photograph of a Packaged Focal Plane InSb CID Array.

SECTION IV. ELECTRONIC TEST CIRCUITS

1. Introduction

A block diagram of the InSb array evaluation system is shown in Figure 22. The InSb array and the silicon scanners, which contain the MOSFET preamplifier and reset switch, are mounted on the cold finger of a cryogenic dewar and operated at a temperature of $77^{o}K$. The remaining peripheral electronic circuits for testing the InSb arrays are mounted in a separate circuit card rack located outside the dewar. In the early stage of the program, the peripheral circuits were partitioned into four circuit boards. They were the element and row timing circuits, column timing circuits, driver and bias circuits, and the amplifier and sample-and-hold circuits. CMOS devices were used for the timing circuits and MOSFET devices were used for the driver circuits. New circuits using TTL devices have since been developed, and they are partitioned into only two circuit boards. One board contains the timing, bias, and driver circuits and the other contains the amplifier and sample-and-hold circuits. Both versions are described below.

2. Timing Circuits (CMOS Version)

The circuits shown in Figure 23 consist of a master clock, element and row timing circuits, and control flip-flop circuits. CMOS devices are used for the timing circuits. The V_{DD} pin is connected to ground and the V_{SS} pin is connected to -12 volts. Thus, the voltage swing is from ground to -12 volts. The master clock is an RC-oscillator, consisting of two inverters (Z16), two resistors, a capacitor and a potentiometer to adjust the oscillator frequency. The buffered output of the oscillator serves as the clock pulse for the element timing circuits.

The element timing circuits consist of a 12-bit shift register, decoding gates and control flip-flops. Two Hex D flip-flops, (Z_1 and Z_2) are connected as a 12-bit shift register. Decoding gates are connected to the output of the first eleven stages of the shift register and monitor their state. When all of the outputs connected to the decoding gates are

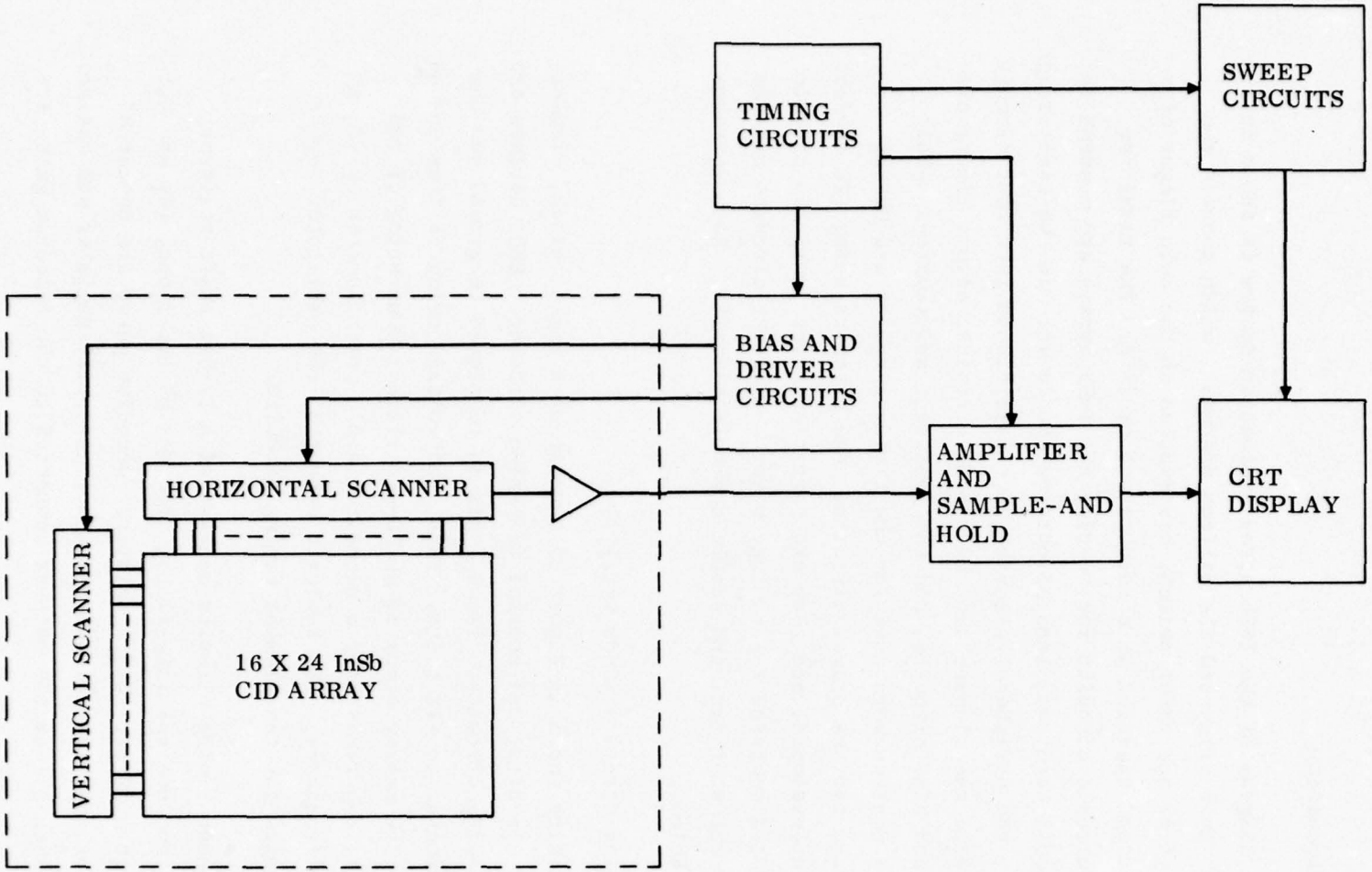


Figure 22. Block Diagram of Array Evaluation System, Displaying Real-Time Raster Scanned IR Images.

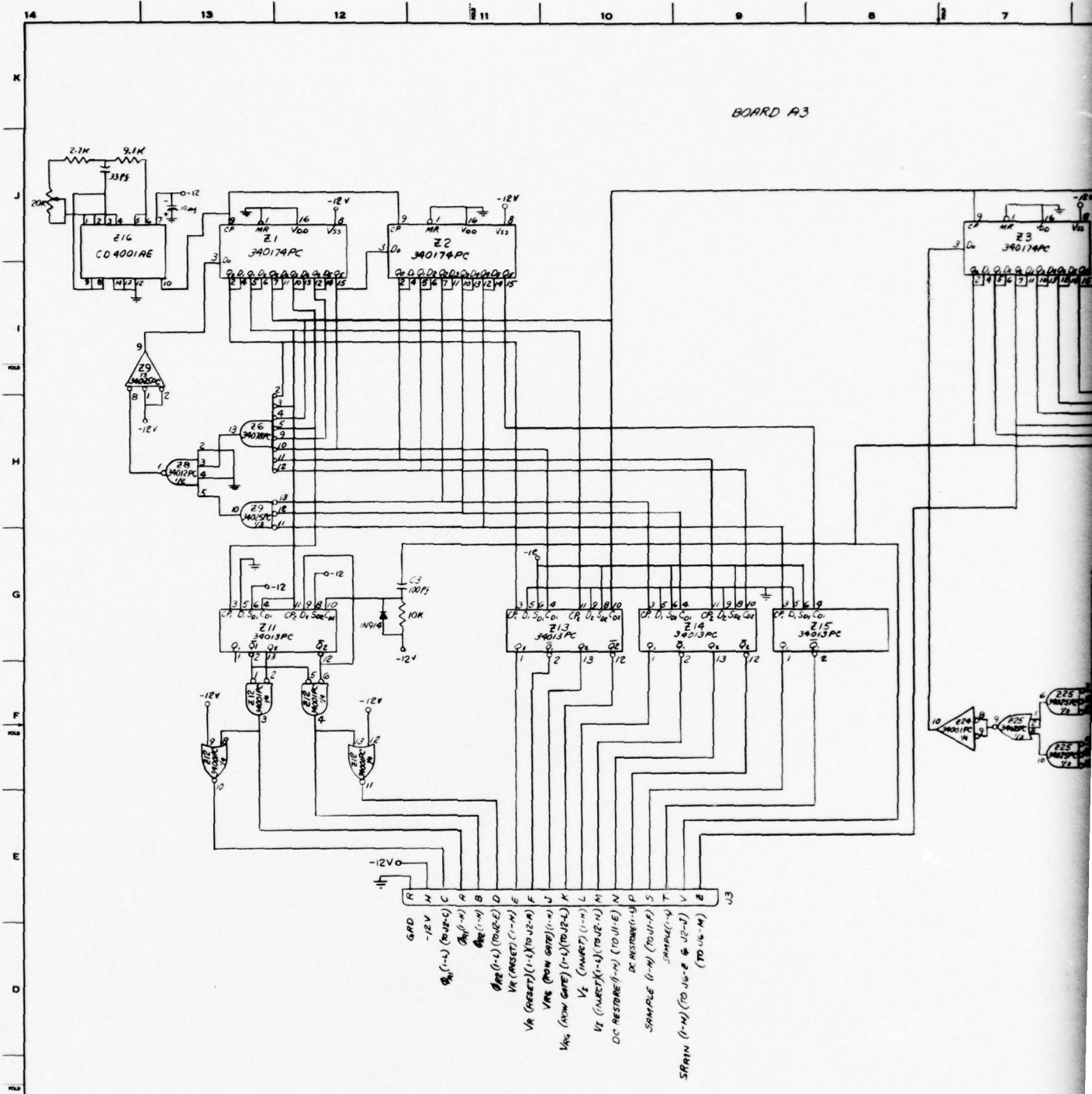
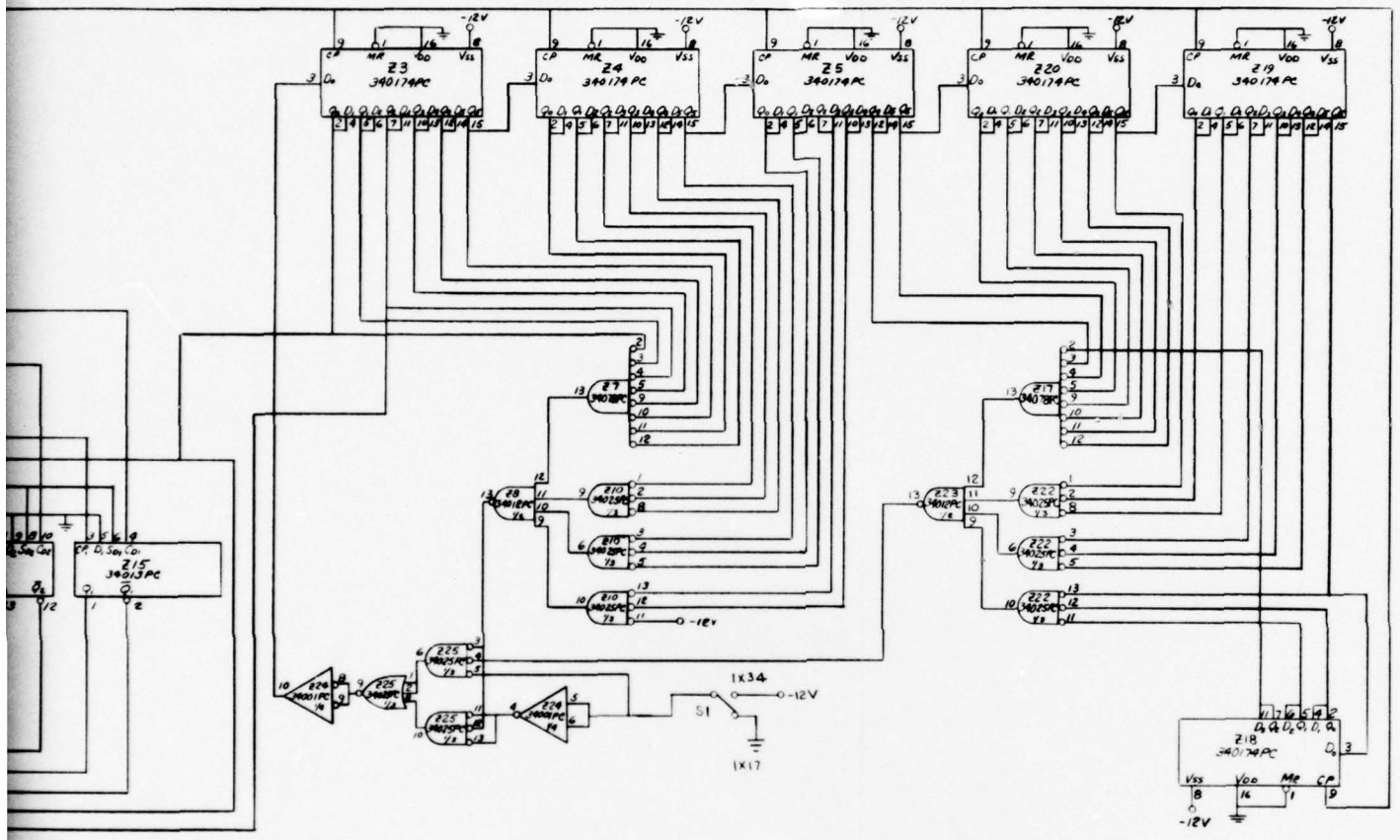


Figure 23. Array Element and Row Timing Circuits (CMOS Version)

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ADDED S1	4/24/77	

BOARD A3



NOTE: PIN 14 = GND, PIN 7 = -12V ON Z6 THRU Z17 & Z22 THRU Z25

ing Circuits (CMOS Version)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON 2-PLACE DECIMALS ± 3-PLACE DECIMALS ± ANGLES ± FRACTIONS ± MATERIAL	ALL SURF. ✓	SIGNATURES	GENERAL ELECTRIC E-LAB SYRACUSE
			IN S4 CID ELEMENT & ROW TIMING CIRCUITS
			SIZE E · CODE IDENT NO. 13688 · SKS6157-E207-133 · SCALE · SHEET

2

"low", a "high" level pulse is generated and applied to the input of the first stage of the shift register. The pulse is shifted through the register. When the decoding gate inputs are all "low", another pulse is generated and applied to the input of the shift register. This process repeats and serves as the element timing function. The dc restore, inject (V_I), sample, row gate (V_{RG}), reset (V_R), Φ_{R1}, Φ_{R2} pulses are generated by controlling the states of the dual D flip-flops (Z11, 13, 14, 15) with the pulse shifted through the element timing shift register. The output from the third stage of the 12-bit shift register is used as the clock pulse for the row timing circuits.

The row timing circuits are similar to the element timing circuits, the only difference being the number of shift register stages and decoding gates. The row timing circuits contain six Hex D flip-flops (Z3, 4, 5, 18, 19 and 20) connected as a 34-bit shift register. Decoding gates are connected to the output of the first 33 stages of the shift register and monitor their state. When all of the outputs connected to the decoding gates are "low", a "high" level pulse is generated and applied to the input of the first stage of the shift register. This pulse is shifted through the register. When the decoding gate inputs are all "low", another pulse is generated and applied to the input of the shift register. This process repeats and serves as the row timing function. The output of the first stage of the shift register is used as the clock pulse for the column timing circuit. It is also inverted and applied to the input of the row silicon scanner located in the dewar. The last 18 bits of the 34 stage shift register are used as row (horizontal) blanking pulses when the 16 elements of the 16x24 array are scanned with the row scanner in this mode of operation.

The above row timing operation takes place when switch S1 is in the 1x34 position. When S1 is in the 1x17 position, the state of the first 16 stages of the shift register determines when a "high" level pulse is applied to the input of the shift register. When the output of the first 16 stages of the shift register is "low", the decoding gates generate and apply a "high" pulse to the input of the first stage of the shift register.

The pulse is shifted through the register. When the inputs of the decoding gates connected to the first 16 stages are all "low", another pulse is generated and applied to the input of the shift register. This process repeats and serves as the row timing function. One bit of the shift register (the 17th) is used as the row (horizontal) blanking pulse when the 16 elements of the 16x24 array are scanned with the row scanner in this mode of operation.

The circuits, shown in Figure 24, consist of the column timing circuits and control flip-flop circuits. The column timing circuits are similar to the row timing circuits, the only difference being the addition of the control flip-flops for generation of the Φ_{C1}, Φ_{C2}, and the column gate (V_{CG}) pulses. The column timing circuits contain six Hex D flip-flops connected as a 34-bit shift register. Decoding gates are connected to the output of the first 33 stages of the shift register and monitor their state. When all of the outputs connected to the decoding gates are "low", a "high" level pulse is generated and applied to the input of the first stage of the shift register. This pulse is shifted through the register. When the decoding gate inputs are all "low", another pulse is generated and applied to the input of the shift register. This process repeats and serves as the column timing function. The output of the first stage of the 34-bit shift register is inverted and applied to the input of the column silicon scanner located in the dewar. The last 10 bits of the 34 stage shift register are used as column (vertical) blanking pulses when the 24 elements of the 16x24 array are scanned with the column scanner in this mode of operation.

The above column timing operation takes place when S2 is in the 1x34 position. When S2 is in the 1x17 position, the column shift register operates the same way as the row shift register does when S1 is in the 1x17 position. Since there are 24 elements in this direction, S2 is placed in the 1x34 position.

The Φ_{C1}, Φ_{C2}, and column gate (V_{CG}) pulses are generated by controlling the states of the dual D flip-flop (Z11 and Z13) with the pulse shifted through the row timing shift register.

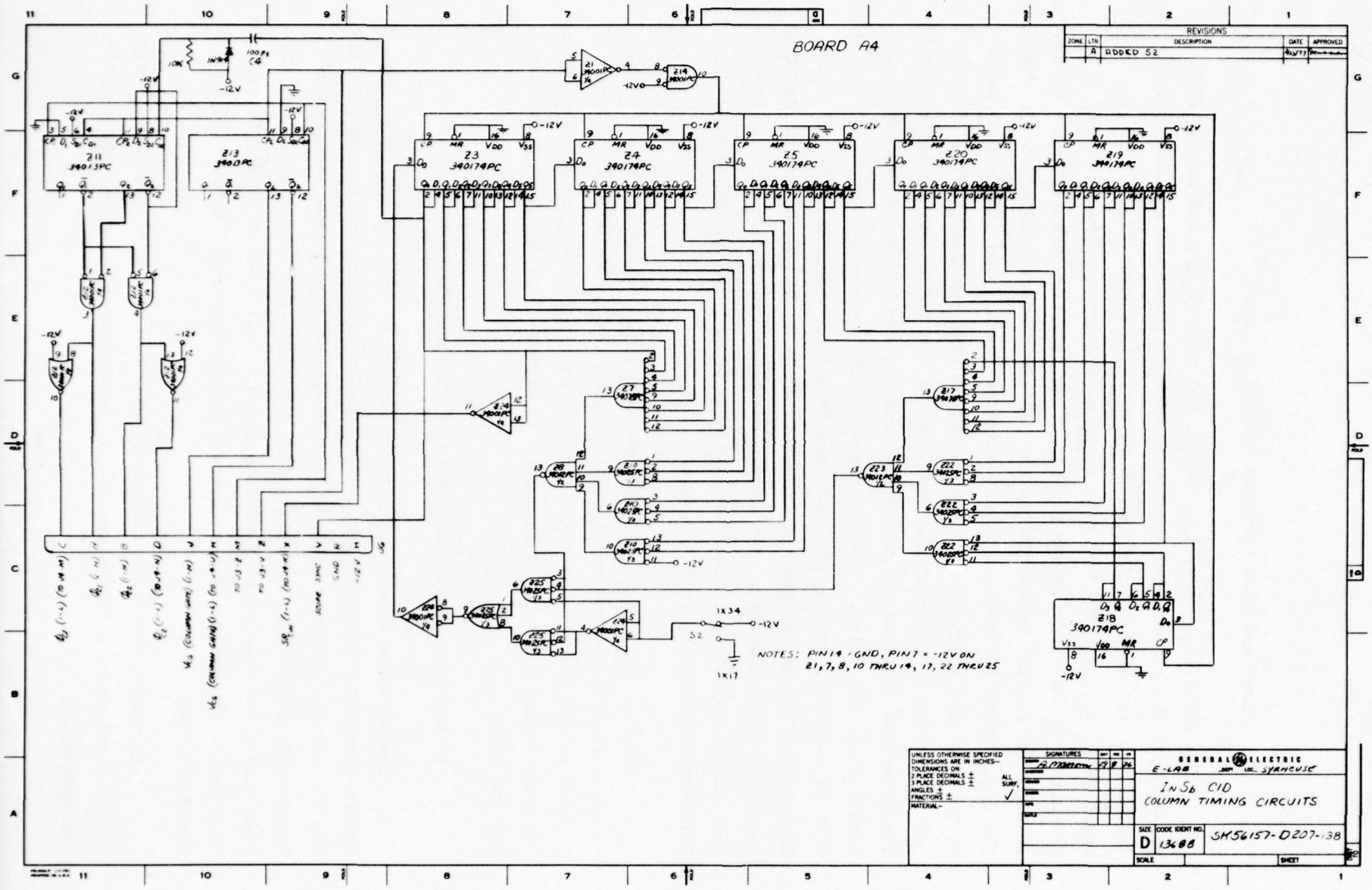


Figure 24. Column Timing Circuits (CMOS)

3. Driver and Bias Circuits (MOSFET Version)

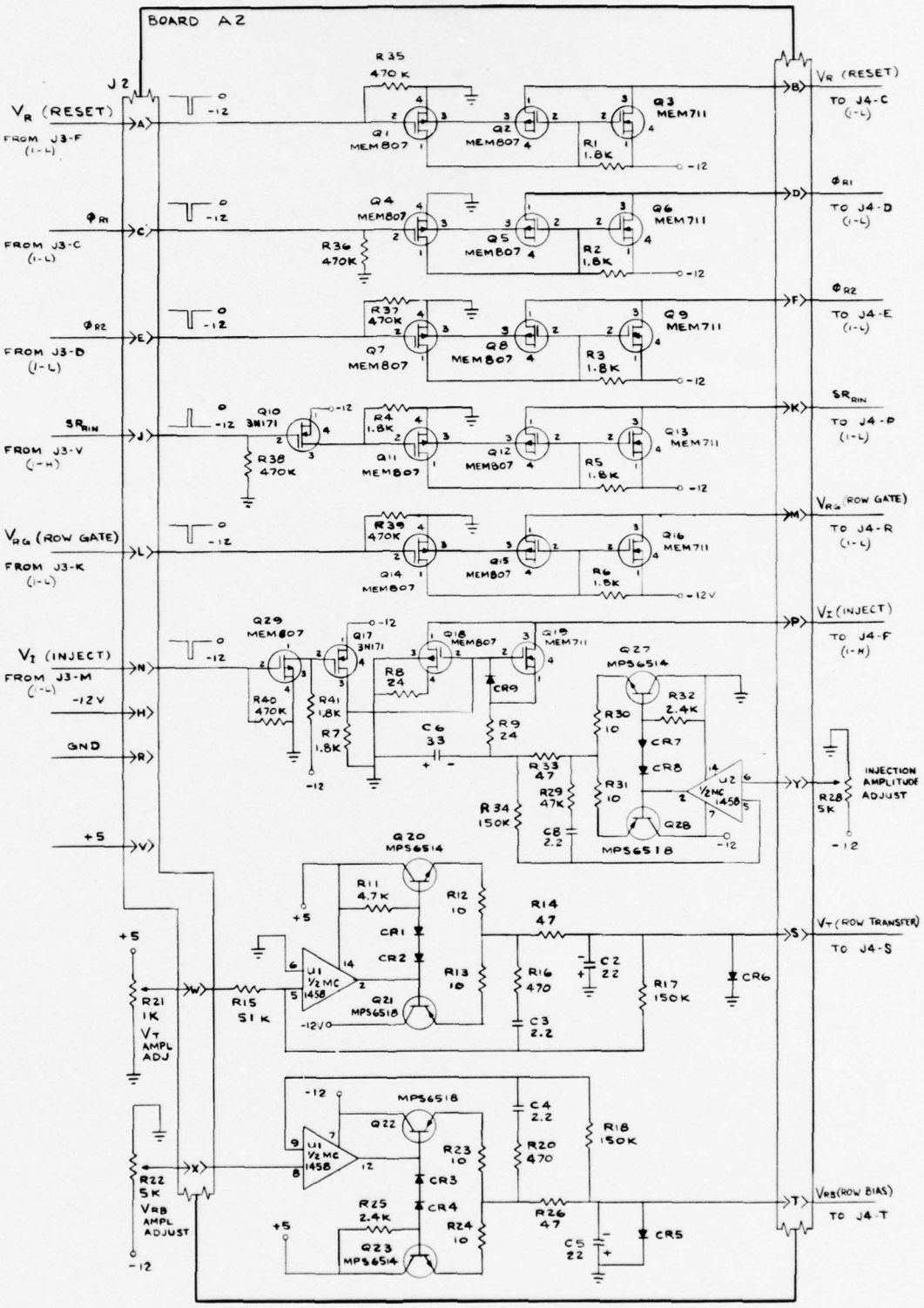
The reset (V_R), Φ_{R1}, Φ_{R2}, SR_{RIN}, row gate (V_{RG}), and inject (V_I) pulses from the element and row timing circuit board are applied to the driver and bias circuit board which is shown in Figure 25. The SR_{RIN}, reset (V_R), Φ_{R1}, Φ_{R2} and row gate (V_{RG}) pulses are applied to MOSFET driver circuits. These circuits are capable of driving the high frequency pulses through the coaxial cables to the row silicon scanner located in the dewar. The SR_{RIN} pulse is inverted by its driver circuit. The inject (V_I) pulse is inverted and combined with a dc level so that the amplitude of the inject pulse can be varied. The amplitude of the inject pulse, controlled by the Injection Amplitude Adjust potentiometer, can be varied from approximately -1 to -11 volts. The row transfer and row bias voltages are dc with an amplitude that can be adjusted from approximately -1 to -11 volts. The level of these voltages are controlled by the Row Transfer and Row Bias Amplitude potentiometers. The wipers of the potentiometers are applied to operational amplifiers. The low impedance output of the amplifiers are filtered before going into the dewar.

The Φ_{C1}, Φ_{C2}, SR_{CIN}, and column gate (V_{CG}) pulses from the column timing circuit board are applied directly to the column silicon scanner located in the dewar. The MOSFET drivers were not necessary for the column silicon scanner since the column rate is either 17 or 34 times less than the row rate.

4. New Timing, Bias and Driver Circuits (TTL Version)

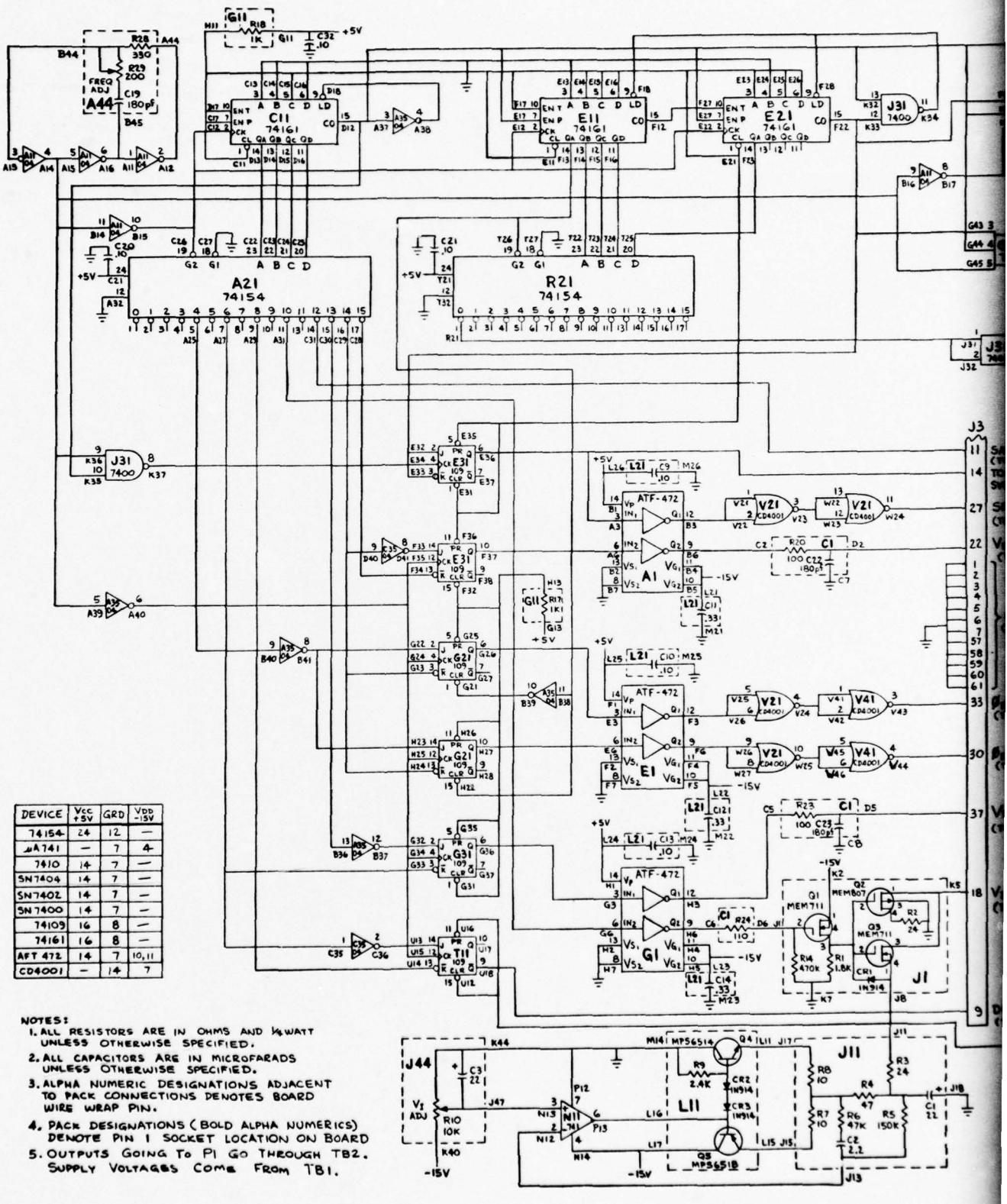
The circuits shown in Figure 26 consist of the timing, bias, and driver circuits. TTL integrated circuits are used for the timing circuits. The TTL voltage levels are translated to MOS voltage levels by means of hybrid thin film integrated circuits. The outputs of these circuits, in most cases, are applied to CMOS integrated circuits which drive the silicon scanners in the dewar. Potentiometers are used to set the bias voltages of the InSb array.

The master clock is an RC-oscillator consisting of three inverters (A11), a resistor, a capacitor, and a potentiometer to adjust the oscillator frequency.



NOTES:
1. ALL DIODES ARE IN 4153, IN4154 OR IN914
2. ALL RESISTORS ARE IN OHMS ± ¼W, 5% UNLESS OTHERWISE SPECIFIED
3. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED
4. R28, R21, R22 MOUNTED REMOTELY (ON CHASSIS)

Figure 25. Clock Drivers and Bias Circuits



DEVICE	Vcc +5V	GRD	VDD -15V
74154	24	12	—
µA741	—	7	4
7410	14	7	—
SN7404	14	7	—
SN7402	14	7	—
SN7400	14	7	—
74109	16	8	—
74161	16	8	—
AFT 472	14	7	10, 11
CD4001	—	14	7

NOTES:

1. ALL RESISTORS ARE IN OHMS AND ¼ WATT UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
3. ALPHA NUMERIC DESIGNATIONS ADJACENT TO PACK CONNECTIONS DENOTES BOARD WIRE WRAP PIN.
4. PACK DESIGNATIONS (BOLD ALPHA NUMERICS) DENOTE PIN 1 SOCKET LOCATION ON BOARD
5. OUTPUTS GOING TO P1 GO THROUGH TB2. SUPPLY VOLTAGES COME FROM TB1.

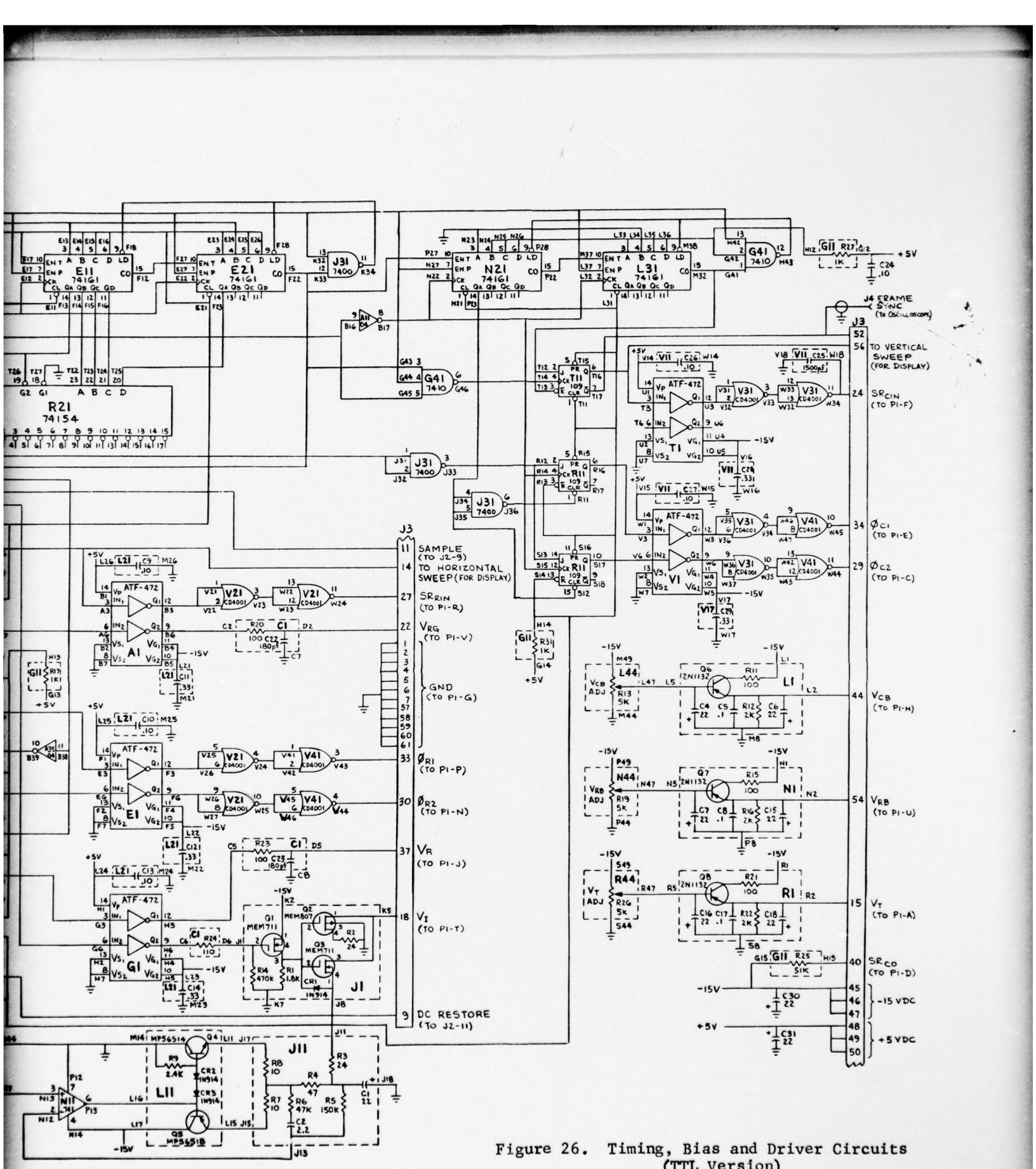


Figure 26. Timing, Bias and Driver Circuits (TTL Version)

The element timing circuits consist of a 4-bit counter (C11) which is pre-loaded, by means of inputs A, B, C and D, to a count of four. The element counter increments its count every time it receives a clock pulse. When the counter reaches a count of 15 (its 16th state), a positive pulse is present on its output. This pulse is inverted and applied to the load input (pin 9) of the counter and the counter is loaded to a count of 4 when the next clock pulse occurs. This process repeats and serves as the element timing function. Thus, each element time is divided into 12 parts. The outputs of the element counter are applied to a 1-of-16 decoder (A21), which is used to decode the state of the element counter by having a low level voltage on only one of its sixteen output pins. Since the element counter is pre-loaded to a count of four, the decoder will only decode counter states 4 to 15. The output pins which decode states 0 to 3 of the counter will always be high because the counter is programmed to count between states 4 and 15.

The dc restore, reset (V_R), row gate (V_{RG}), and Φ_{R1} and Φ_{R2} row scanner clock pulses are generated by controlling the states of J-$\overline{K}$ flip-flops (E31, G21, G31, and T11) with the appropriate decoded output pulse of the element counter decoder. The sample pulse is obtained by using the decoded output of state 12 of the element timing decoder and the inject pulse is obtained by using the decoded output of state 10 of the element timing decoder.

The Q_A output of E11 is used as a synchronization pulse for the row scanner clock inputs (Φ_{R1} and Φ_{R2}). This pulse is used to clear flip-flop G21 so that the required relationship between the SR_{RIN}, Φ_{R1}, and Φ_{R2} pulses occurs for proper scanner operation.

The row timing circuits are similar to the element timing circuits, the only difference being the number of states of the row counter. The row counters, E11 and E21, are programmed to count 34 states by pre-loading the counters to 222. The row counter increments its count every time it receives a clock pulse coincident with an output pulse from the element counter that is connected to the Enable P inputs of the row counter. When the counter reaches a count of 255 (its 256th state), a positive pulse is

present on its output. This pulse is ANDed with the element counter output pulse, inverted, and applied to the load inputs of the counter. The counter is loaded to a count of 222 when the next clock pulse occurs. This process repeats and serves as the row timing function. The output of the row counter is delayed one bit (one element time) and serves as the input (SR_{RIN}) to the row silicon scanner, located in the dewar.

The column timing circuits are similar to the row timing circuits, the only difference being the addition of the control J-$\overline{K}$ flip-flops for generation of the Φ_{C1} and Φ_{C2} pulses. The column counters, N21 and L31, are programmed to count 34 states by pre-loading the counters to 222. The column counter increments its count every time it receives a clock pulse coincident with the output pulses from the element and row counters applied to the Enable P and Enable T inputs, respectively. When the counter reaches a count of 255 (its 256th state), a positive pulse is present on its output. This pulse is ANDed with the element counter output pulse, inverted, and applied to the load inputs of the counter. The counter is loaded to a count of 222 when the next clock pulse occurs. This process repeats and serves as the column timing function. The output of the column counter is delayed one bit (one row time) and serves as the input (SR_{CIN}) to the column silicon scanner located in the dewar. Since 32-stage silicon scanners are employed to scan the 16x24 array, a 34x34 timing format is used. Thus, the displayed output results in eighteen element blanking periods on the rows and 10 element blanking periods on the columns.

The Φ_{C1} and Φ_{C2} column scanner clock pulses are generated by controlling the states of J-$\overline{K}$ flip-flops (R11) with the appropriate decoded output pulse of row counter decoder R21. The Q_A output of N21 is used as a synchronization pulse for the column scanner clock inputs (Φ_{C1} and Φ_{C2}). This pulse is used to clear flip-flop R11 so that the proper relationship between the SR_{CIN}, Φ_{C1} and Φ_{C2} pulses occurs for proper scanner operation.

The TTL voltage levels of the SR_{RIN}, V_{RG}, Φ_{R1}, Φ_{R2}, V_R, V_I, SR_{CIN}, Φ_{C1} and Φ_{C2} pulses are applied to the inputs of MOS data level converters. These units (ATF-472) can be directly driven by standard TTL circuits. The output voltage of the level converters is 0 to -15 volts. The SR_{RIN}, Φ_{R1},

Φ_{R2}, SR_{CIN}, Φ_{C1} and Φ_{C2} pulses are applied to CMOS devices (CD4001). The V_{DD} pin of the CMOS devices is connected to ground and the V_{SS} pin is connected to -15 volts. Thus, the output voltage swing is from ground to -15 volts. The outputs of the CMOS devices are applied to the row and column silicon scanners located in the dewar. The CMOS devices were necessary because the output impedance of the device is low, in both the logic one and zero states. The ATF-472 device was not used as the driver for the scanners because pick-up problems occurred when its output was at the ground level.

The V_R and V_{RG} pulses from the ATF-472 devices are filtered with a 100 ohm resistor and 180 pF capacitor before going into the dewar. The injection pulse from the ATF-472 is combined with a dc level, by means of Q1, Q2 and Q3, so that the amplitude of the injection pulse can be varied. The amplitude of the injection pulse, controlled by the Injection Amplitude Adjust potentiometer, can be varied from approximately -2 to -13 volts. A timing diagram is shown in Figure 27.

The row transfer (V_T), row bias (V_{RB}), and column bias (V_{CB}) voltages are dc voltages which can be adjusted from approximately 0 to -14 volts. The values of the voltages are controlled by potentiometers R26, R19, and R13, respectively. The wipers of these potentiometers are applied to the bases of emitter-follower transistors Q6, Q7 and Q8. The low impedance output of the emitter-followers are filtered before going into the dewar.

The column silicon scanner output pulse (SR_{CO}) can be used to monitor the operation of the column silicon scanner in the dewar. If the scanner is operating properly, a positive pulse at the frame rate will be present at the SR_{CO} test point located on TB-2. A row silicon scanner output pulse is not used to monitor the operation of the row scanner. It is checked at room temperature and normally operates at the low temperature without any problems.

5. Amplifier and Sample-and-Hold Circuits

The amplifier and sample-and-hold circuits are shown in Figure 28. A differential preamplifier scheme is used so that the common mode rejec-

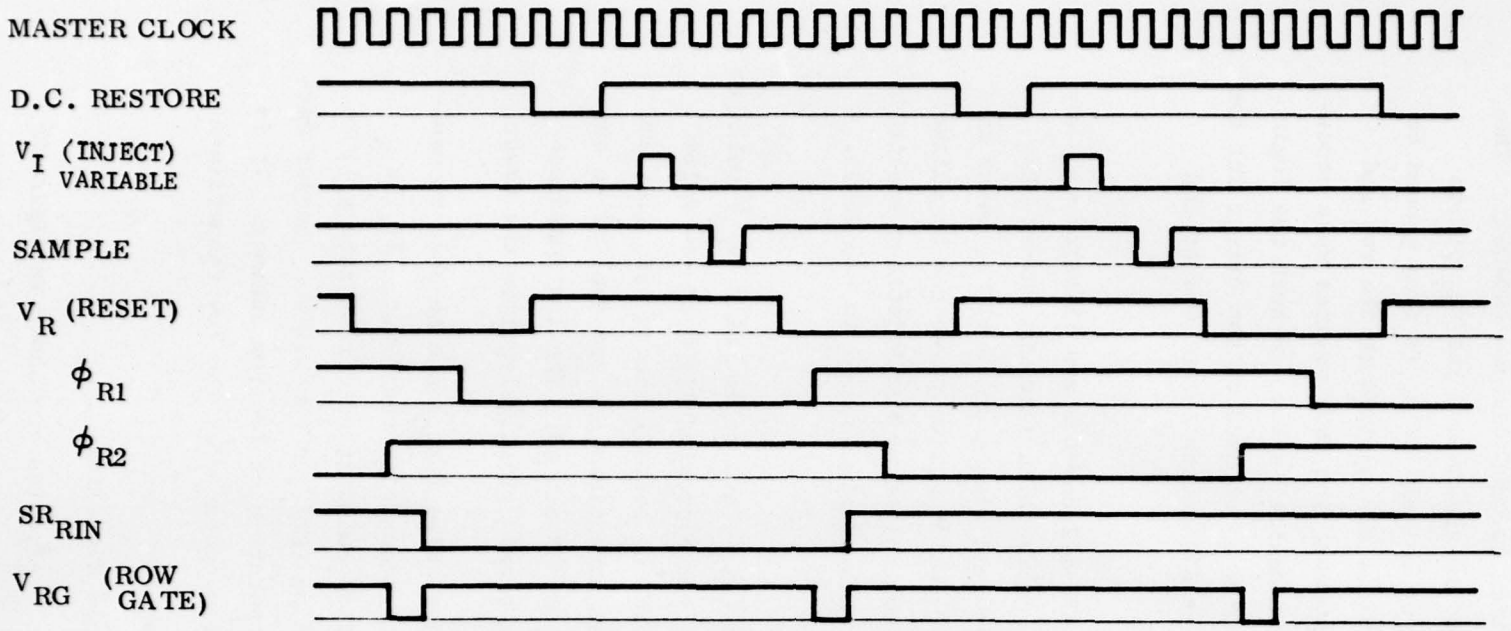


Figure 27a. Element and Row Timing Diagram

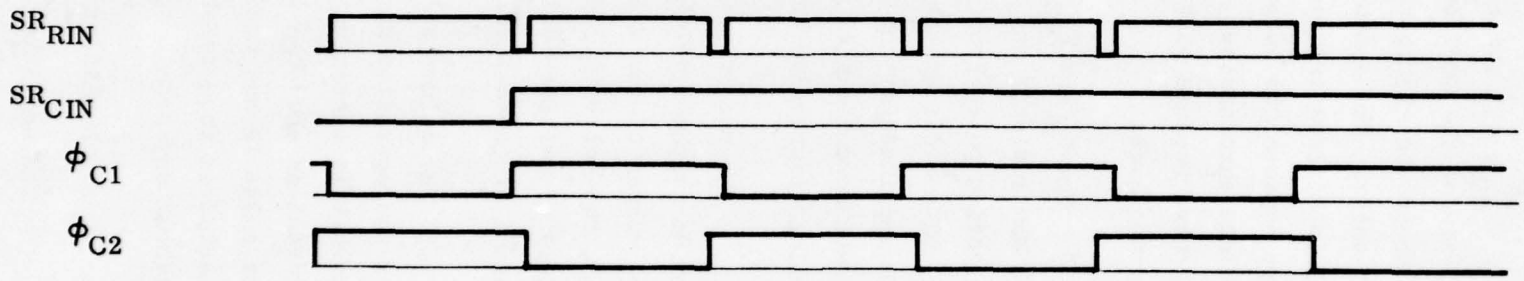
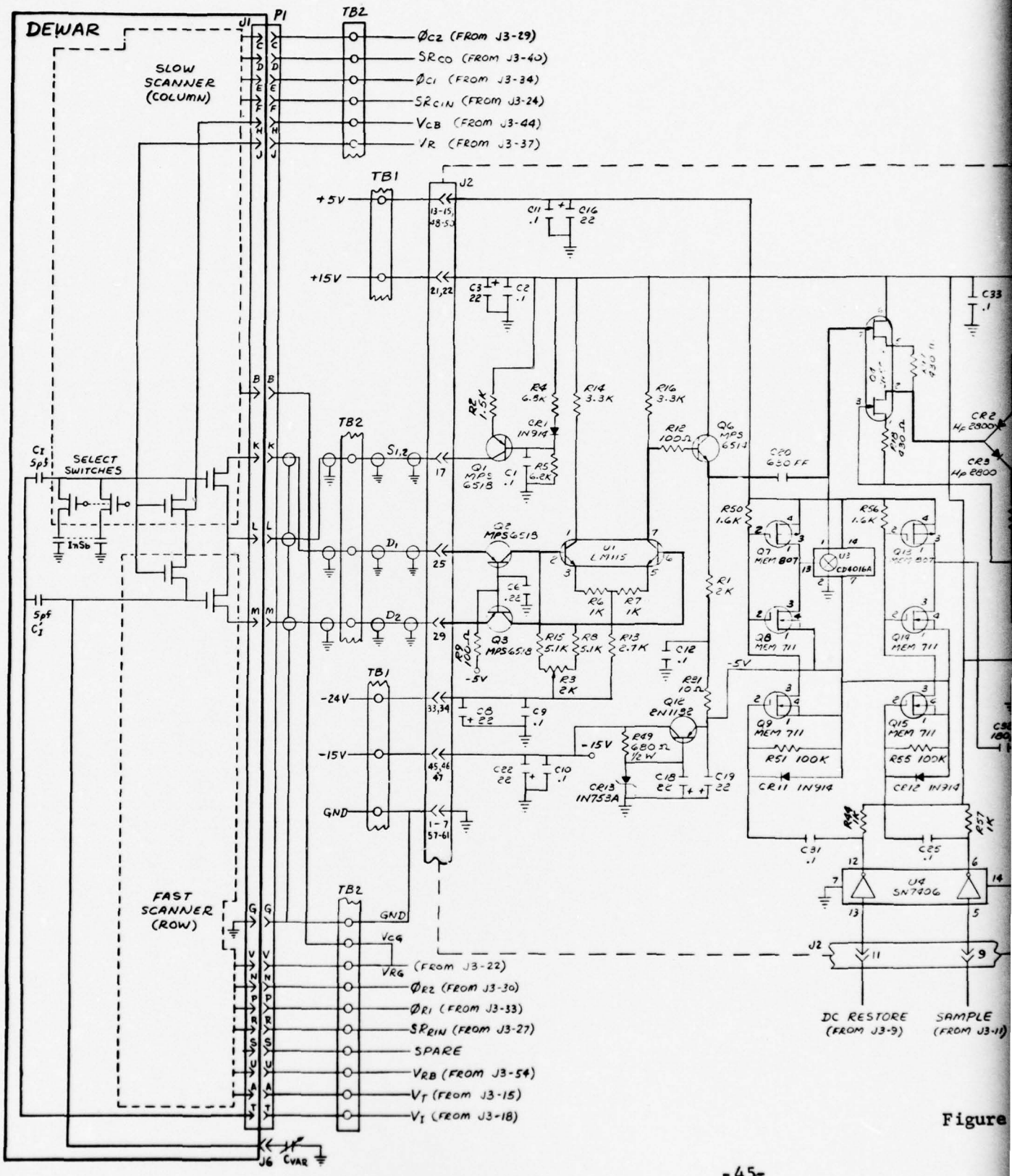


Figure 27b. Column Timing Diagram


DEWAR
J1
P1
TB2
ØCZ (FROM J3-29)
SRCO (FROM J3-40)
ØCI (FROM J3-34)
SRCIN (FROM J3-24)
VCB (FROM J3-44)
VR (FROM J3-37)
SLOW SCANNER (COLUMN)
TB1
J2
+5V
+15V
C11 .1
C16 22
C3 22
C2 .1
C33 .1
R2 1.5K
R4 6.8K
R14 3.3K
R16 3.3K
CR1 IN914
Q1 MPS 6518
C1 .1
R5 6.2K
R12 100Ω
Q6 MPS 6514
C20 680 PF
CR2 HP 2800
CR3 HP 2800
R50 1.6K
R56 1.6K
Q7 MEM 811
U3 CD4016A
Q13 MEM 811
C1 5pf
SELECT SWITCHES
InSb
S1,2
D1
D2
Q2 MPS6518
U1 LM115
C6 .22
R6 1K
R7 1K
R1 2K
Q3 MPS6518
R15 5.1K
R8 5.1K
R13 2.7K
R3 2K
R10 100Ω
-5V
C12 .1
R11 10Ω
Q12 2N1132
Q8 MEM 811
Q14 MEM 811
Q9 MEM 811
Q15 MEM 811
R51 100K
R55 100K
CR11 IN914
CR12 IN914
-24V
-15V
GND
C8 22
C9 .1
C22 22
C10 .1
R49 680Ω 1/2 W
CR13 IN753A
C18 22
C19 22
R54 1K
R57 1K
C31 .1
C25 .1
U4 SN7406
FAST SCANNER (ROW)
VCG
VRG (FROM J3-22)
ØR2 (FROM J3-30)
ØR1 (FROM J3-33)
SRIN (FROM J3-27)
SPARE
VRB (FROM J3-54)
VT (FROM J3-15)
VI (FROM J3-18)
J6
CVAR
DC RESTORE (FROM J3-9)
SAMPLE (FROM J3-11)

Figure

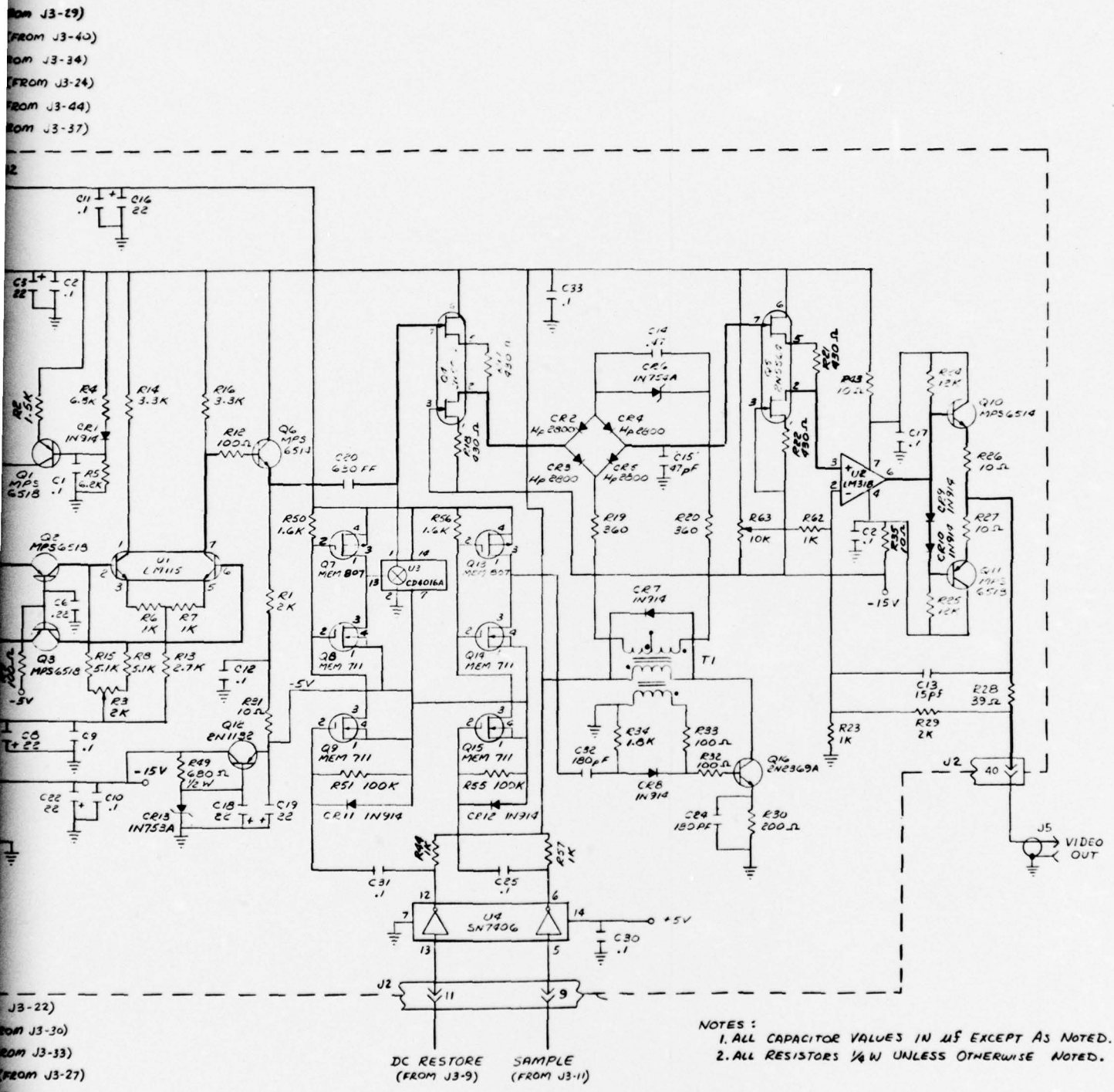


Figure 28. Amplifier and Sample-and-Hold Circuits

tion properties of the differential preamplifier eliminate the effects of the large injection and reset (V_R) pulses. The injection pulse is ac-coupled to the array through a 5 pF capacitor (C_I) located in the dewar. The injection pulse is also ac-coupled to a variable capacitor (C_{VAR}), located outside the dewar, through a 5 pF capacitor (C_I') located in the dewar. The InSb array is connected, via the enable line, to the gate of a MOSFET transistor located on the column scanner, and the variable capacitor, C_{VAR}, is connected to the gate of a MOSFET transistor located on the row scanner. The sources of these MOSFETs are connected together to a current source, Q1, which supplies approximately 2 mA of current to each MOSFET. The drain of the column scanner MOSFET, D1, is connected to the emitter of Q2 and the drain of the row scanner MOSFET, D2, is connected to the emitter of Q3. The combination of the MOSFETs and common base transistors Q2 and Q3 form two cascode amplifiers. The cascode amplifier exhibits low noise and wide bandwidth characteristics which are ideal for this application. Also, the common-base configuration of Q2 and Q3 has a low input impedance, so the transition from the drains of the MOSFETs in the dewar to the emitters of Q2 and Q3 on the circuit board by means of coaxial cable poses no problems.

Resistors R15, R18, and potentiometers R3, which are connected to the collectors of Q2 and Q3, serve as the load resistors for the cascode configuration. The gain of each cascode stage is approximately $g_m R_L$. The MOSFET's have a W/L ratio of 44/.3 and a g_m of 2000 μmhos at 300°K with a drain current of 2 mA. The g_m increases to 5000 μmhos when the temperature of the MOSFETs is 77°K. Thus, the gain of each cascode stage is approximately 30. The collectors of Q2 and Q3 are connected to the bases of a matched dual monolithic transistor pair (U1). U1 is connected as a differential amplifier stage and has a gain of 1.5. The output of the differential amplifier is applied to a buffer transistor (Q6). The emitter of the buffer transistor is applied to the dc restore capacitor (C20).

The other side of C20 is connected to one gate of a dual JFET, which is connected in a source follower configuration, and to the input of a bilateral transmission gate (pin 1 of U3). The dc restore pulse, from J3-9,

is level shifted from a TTL level to a 0 to +15 volt level by U4. The output of U4 is ac-coupled to the gate of Q9. MOSFETs Q7, Q8, and Q9 level shift the dc restore pulse to a +5 to -5 volt level so that the control input of the transmission gate is at the proper voltage. When the dc restore pulse is present, the transmission gate turns on and connects one side of the dc restore capacitor (C20) to ground. The use of a dc restore switch eliminates any kTC noise caused by the reset switch located in the dewar. The output of source follower Q4 is applied to the input of a diode bridge which is part of the sample-and-hold circuit. The sample pulse, from J3-11, is level shifted in the same manner as the dc restore pulse by U4, Q13, Q14 and Q15. The sample pulse is differentiated by C32 and R34 and turns on transistor Q16. Q16 and T1 form a blocking oscillator circuit which has a pulse width of approximately 125 nsec. The secondary of T1 is connected to the sample-and-hold diode bridge. When Q16 is on, the diode bridge is on and allows the output of source follower Q4 to be applied to the hold capacitor (C15) of the sample-and-hold circuit. When Q16 is off, the diode bridge turns off due to the reverse voltage on C14 from zener diode CR6. When the diode bridge is off, the hold capacitor holds its voltage until the next sample pulse occurs.

The hold capacitor is connected to a gate of a dual JFET (Q5) which is connected as a source follower. The input impedance of the source follower is very high so that there is no loss in voltage across the hold capacitor during the hold time. The output of the source follower is applied to the high impedance non-inverting input of the LM318 operational amplifier (U2). U2, Q10, Q11 and associated components for a post-amplifier which has a gain of three. Thus, the total gain of the amplifier is approximately 135. Resistor R62 and potentiometer R63 are used to adjust the dc level of the video output.

Transistor Q12 and its associated components form a voltage regulator. The -15 volt supply is connected to zener diode CR13 through resistor R49. The zener diode is connected to the base of transistor Q12 which serves as the series pass transistor of the voltage regulator.

6. Sweep Circuits

Figure 29 shows the schematic diagram of the sweep circuits used with a Hewlett Packard model #1332A CRT display. A constant current diode is used to supply .47 mA of current to capacitor C_s. The constant current to the capacitor causes the voltage across the capacitor to increase linearly as a function of time. The $\overline{Q}$ outputs of the SR_{RIN} (E31) and SR_{CIN} (T1) flip-flops are ac coupled to the base of the transistor. The transistor turns on when the input is positive and discharges the voltage across C_s. When the positive pulse ceases, the transistor turns off and the voltage across the capacitor starts to increase linearly. The voltage across the capacitor is applied to the sweep inputs of the CRT display. The value of C_s in the horizontal sweep circuit is .047 μF and the value of C_s in the vertical sweep circuit is 1.3 μF.

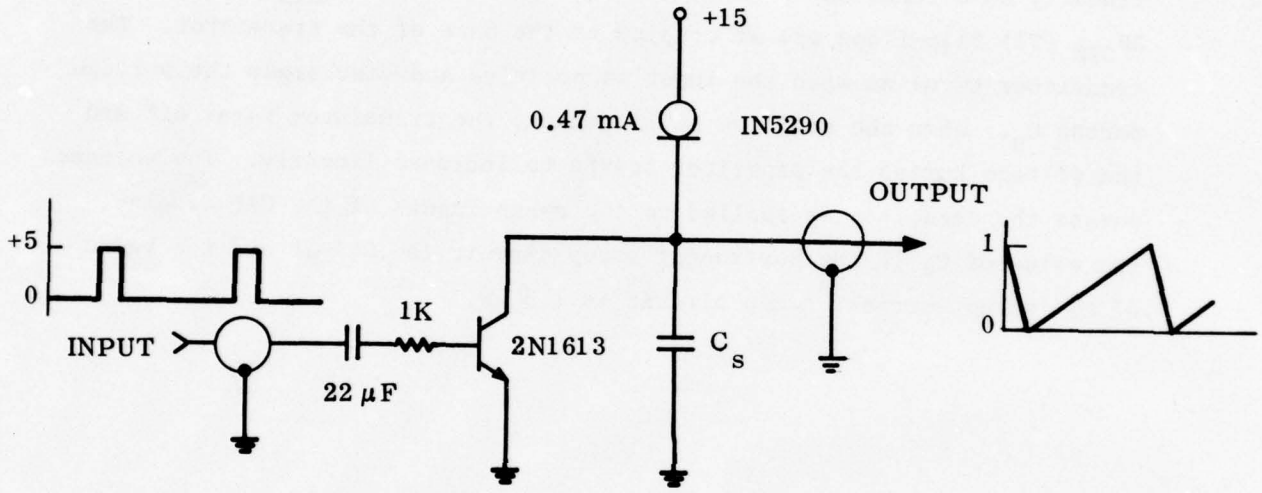


Figure 29. Sweep Circuits Used to Drive a CRT Display Monitor.

SECTION V. EVALUATION AND MEASUREMENTS

1. Test Setup

The demountable cryogenic dewar containing the final packaged array, a lens, and the IR image patterns were mounted in a straight line on a long optical bench. All of the necessary electronic circuits were conveniently located directly behind the dewar. The video output signal was displayed on both an oscilloscope and an X-Y CRT. The main objective here was to demonstrate the two-dimensional mode of operation and to measure the charge transfer between row and column gates in each resolution element.

A special fixture was designed to facilitate mounting of the array package in the dewar[1]. The array can be simply snapped into the fixture socket, which contains all of the necessary lead connections. A holding plate and screw secure the array package down to the cold finger for low-temperature operation, 77°K.

The imaging capabilities of the arrays were tested using a lens to focus the object images on the arrays. Pattern reticles made of aluminum foil were used as the objects. A heater generated an IR object and the imaged output video signal from the array was then displayed on a CRT screen or monitored on a scope. Figure 30 is a block diagram of the array testing setup. A more detailed discussion of the test electronic circuits is presented in Section IV.

2. Test Procedure and Results

Two silicon shift-register scanners are used to sequentially read out the two-dimensional CID arrays as shown in Figure 31. The vertical scanner is used for all of the row lines and the horizontal scanner for all of the column lines. The enable line of the horizontal scanner is connected to the preamplifier. All of the row gates are biased to V_{RB} via the switches controlled by V_{RG}. The column gate bias, V_{CB}, is applied to the gates via the reset and column switches, V_{CG}. The vertical scanner operates at high speed (at an element rate), while the horizontal scanner scans at slow speed (at a line rate). For array interrogation, the

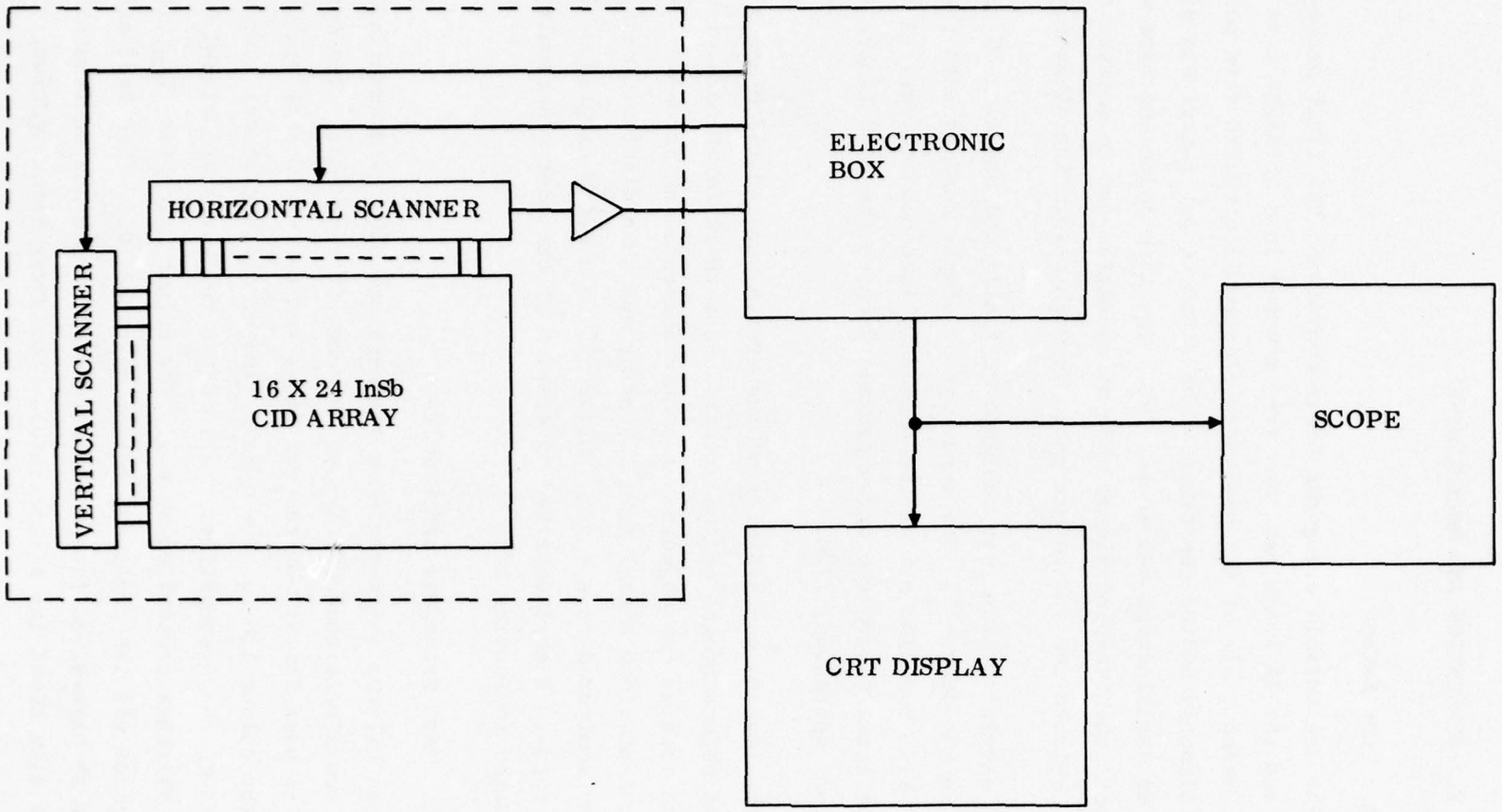


Figure 30. Block Diagram of Array Testing Setup.

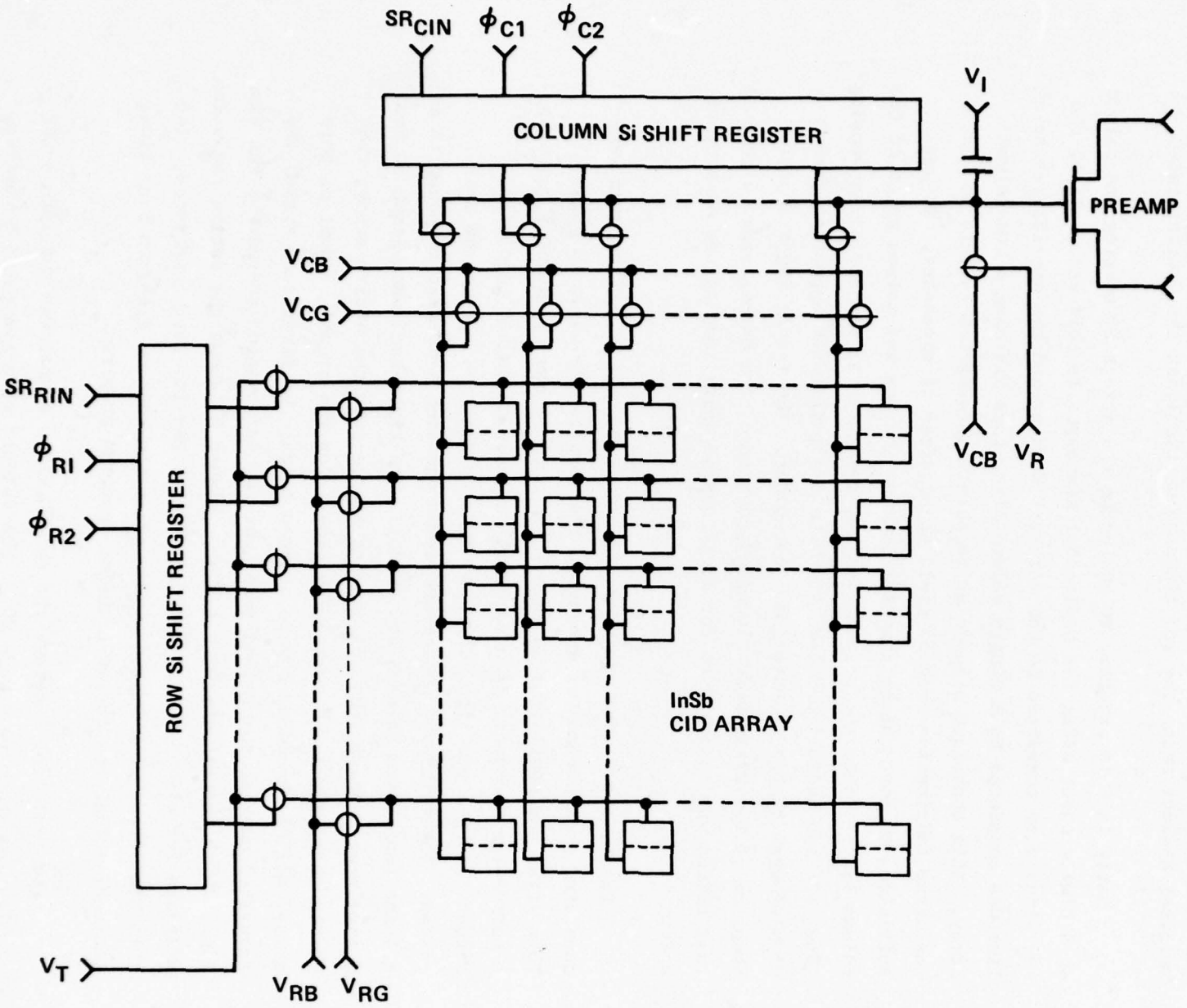


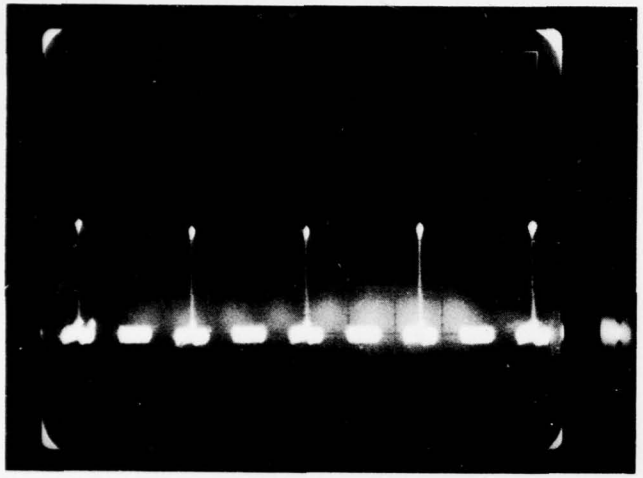
Figure 31. Schematic Diagram of Two-Dimensional InSb CID Focal Plane Array Configuration, Used in a Staring Mode of Operation.

horizontal scanner selects one column at a time at a line rate, and the vertical scanner scans the row lines sequentially at the element rate.

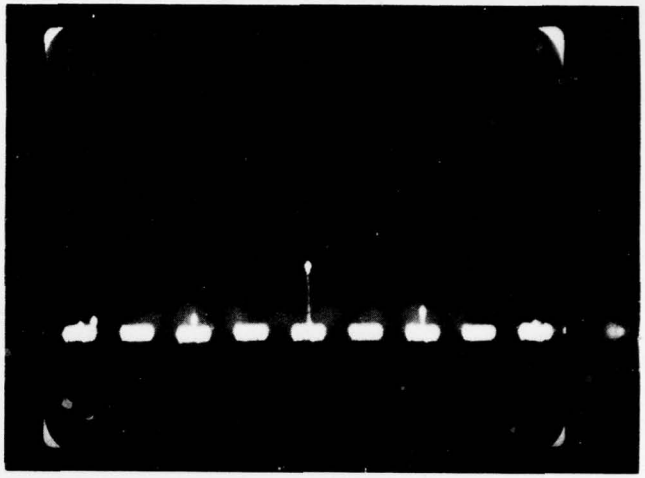
Early in this program, we evaluated the arrays by testing one column at a time without using the horizontal scanner. In this case, all of the row lines were connected to the vertical scanner and the amplifier-sensing line was connected to a single column line, thus yielding a one-column array. This technique allowed us to obtain information quickly so that the array fabrication process could be adjusted if necessary. It was sufficient to test charge transfer between the row and column gates of the column line. Since the column line was connected to the amplifier sensing line, at each injection pulse the output signal would appear at every element when charge transfer did not occur. The result might appear, then, as if the array were blooming; therefore, the output video signal of that column was observed on the oscilloscope while imaging one element at a time.

Later, after some progress had been made, all of the columns were connected to a horizontal scanner. The results are shown in Figure 32. This array was configured so that there were 24 row lines and 16 columns. A narrow-line object (heated wire) was focused on one resolution element along a row line, corresponding to a single element on every column. The left-hand photograph shows the single-element response in all columns (only five columns are shown). The right-hand photograph is for a single-element response of a point source over the entire array; the bottom photo shows the no-imaging case. For the signal readout of this array, all of the columns were scanned twice; the first scan erased the saturated charge; the second read out the information stored for the line time, which was set at about 1.5 ms. Figure 33 shows the entire raw video displays for all of the 12 columns (out of the 16) that functioned. Note that the output of unimaged elements was constant on a common base line, indicating that the charge transfer occurred properly.

For real time imaging, the output video signal was fed into a CRT display, as shown in Figure 30. The objects were generated by cutting patterns in aluminum foil and a lens focused the patterns on the array in

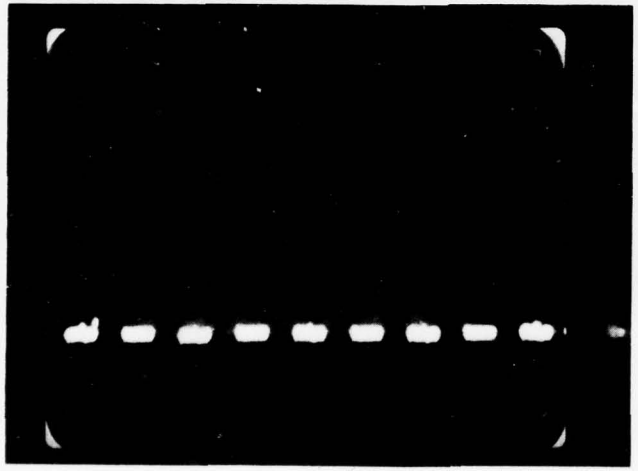


RESPONSE TO LINE IMAGE



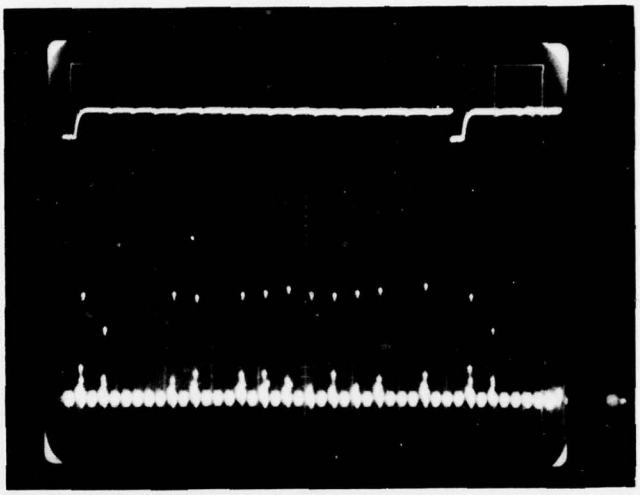
SINGLE ELEMENT RESPONSE TO POINT IMAGE

RESPONSE TO NO IMAGE



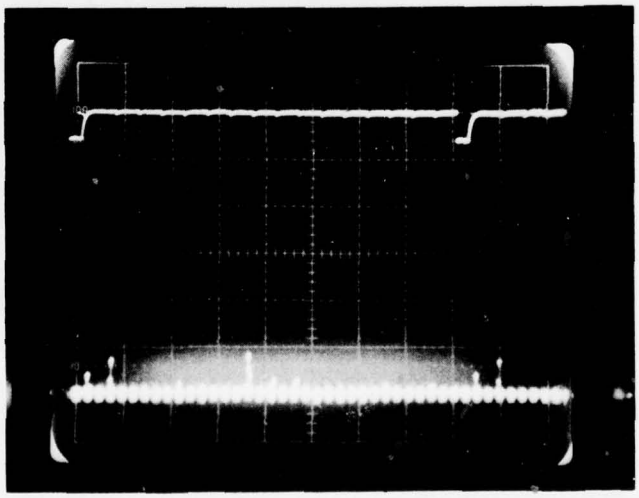
SCALE:
VERT. 1 VOLT/DIV;
HORIZ. 2 ms/DIV.

Figure 32. Displays of Raw Video Signal on an Oscilloscope.



RESPONSE TO LINE IMAGE

SCALE:
VERT. 1V/DIV
HORIZ. 5 ms/DIV



RESPONSE TO NO IMAGE

Figure 33. Raw Video Displays of All Columns, Revealing Complete Video Signal Information (Signal plus Pattern Noise). The 12 out of 16 Columns Are Operational.

the dewar. Behind the object cutouts, a heater produced IR patterns. All of this test equipment was mounted on a common optical bench; the lens was mounted on a three-dimensional movable holder for fine control of the object focus. Typical output video displays of an array are shown in Figure 34. In this case, the object patterns were a cross an an X. The extra bright lines shown are due to the fact that these arrays were scanned in a 34x34 format, but the array contains only 16x24 elements. The line from lower right to upper left is an unblanked CRT retrace. The integration time of this measurement was about 2 ms. The operation of another array is shown in Figure 35. In these photos, the reticle patterns, USA, GE and NRL, are clearly imaged on the CRT monitor; they are as clear as the object patterns, indicating good two-dimensional array operation. The image displays of additional reticle patterns are shown in Figure 36. The bottom picture was obtained by using a negative reticle of the middle picture pattern. Note that the imaged edge definition, again, is very sharp, revealing a good modulation transfer characteristic. Figure 37 shows a video display of a fully irradiated output and the image of a soldering iron tip, respectively. In the top photo, all 16x24 elements are displayed; the bottom photo shows sharp edge definition of the hot soldering iron tip. There is no sign of blooming in the column line direction, even with this relatively hot source, indicating a good charge transfer. The above array evaluation was not intended as a measure of sensitivity, but to demonstrate two-dimensional array operation. As shown, the array operates successfully, even with a relatively hot source ($\approx 300^{o}C$). It should also be noted that the displays described above were done with a raw video signal. To obtain better image quality, and/or fine gray scale images, some signal conditioning, such as frame-to-frame comparison or a simple computer technique, must be used.

In an independent program conducted within GE, we have shown that digital computer signal processing does enhance image quality considerably. Figure 38 is a schematic diagram of a 1x32 focal plane line array; a typical output signal for all 32 elements, uniformly irradiated, is shown in the insert. Typical uniformity data for such a line array are shown in Figure 39. The responsivity variation is in the range of 2.5%

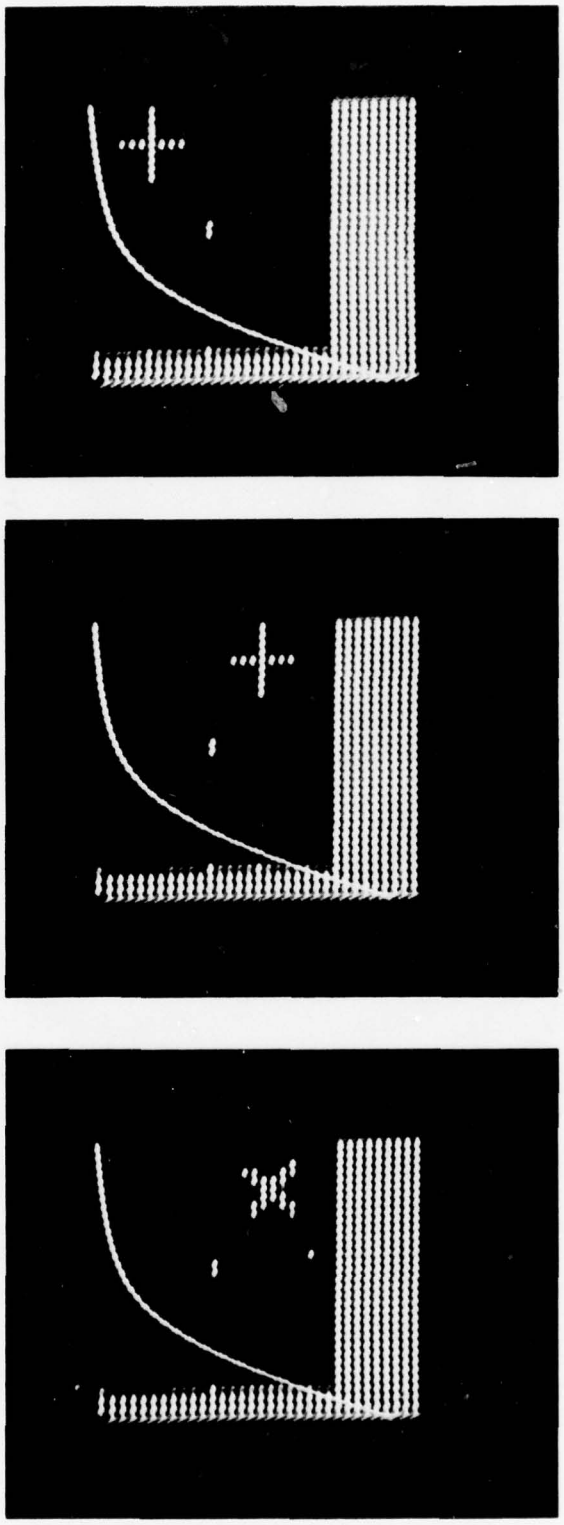


Figure 34. Raw Video Image Displays of Simple Object Patterns on a CRT Monitor Obtained with a 16x24 InSb CID Array

Figure 35. Image Displays of "Word" Reticle Patterns, Obtained with Another 16x24 InSb CID Imager. The Displays Are as Clear as the Object Patterns.

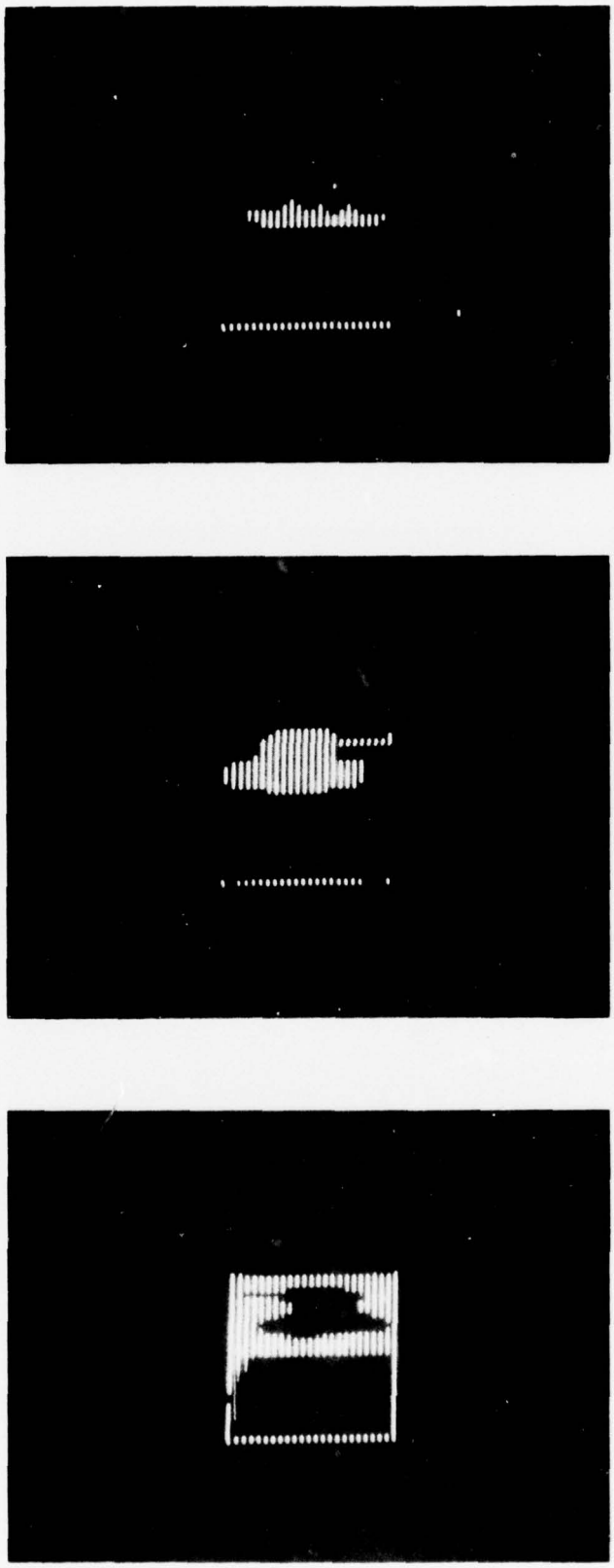
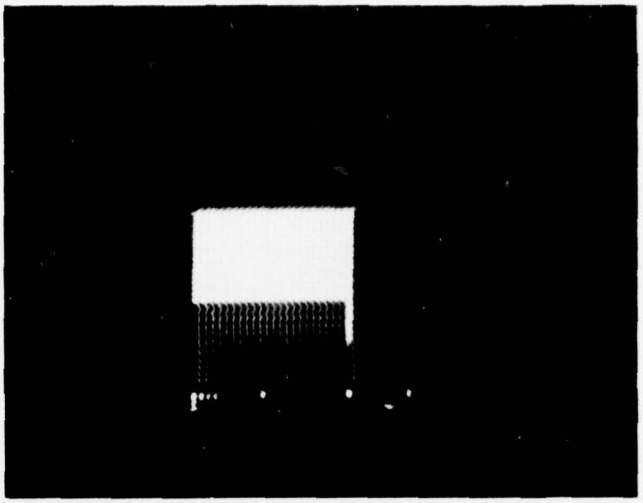


Figure 36. Image Pictures of "Shape " Reticle Patterns, Obtained with the Same Array Shown in Figure 35.



FULL IRRADIATION

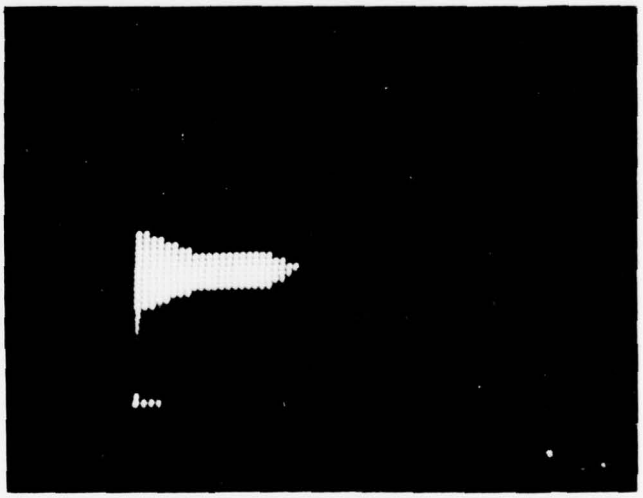


IMAGE DISPLAY OF A HOT SOLDERING IRON TIP

Figure 37. Additional Video Displays of the Same Array Shown in Figure 35. There Is No Sign of Blooming in the Column Lines for the Image of Solder Ion Tip, Indicating a Good Charge Transfer.

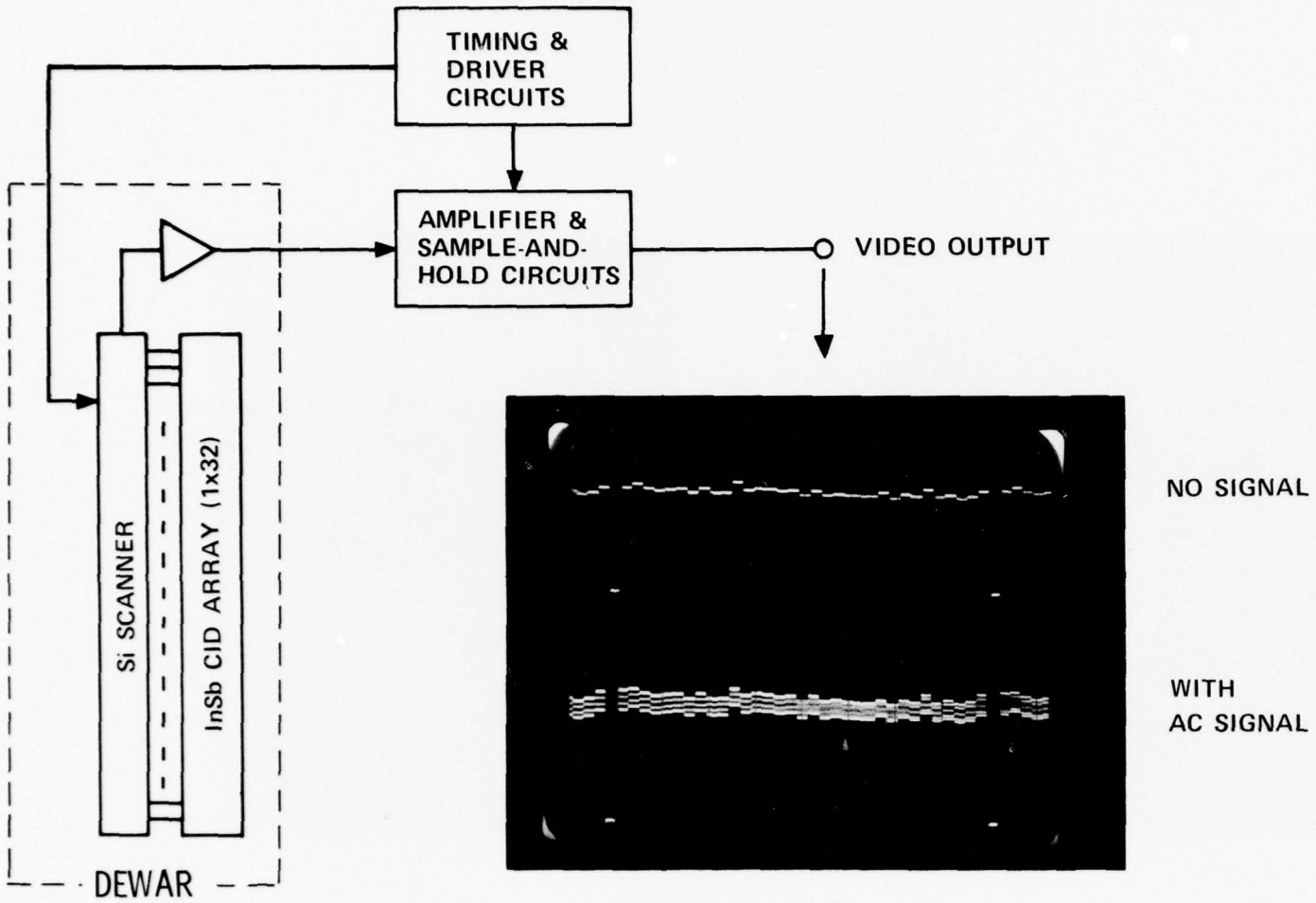


Figure 38. Schematic Diagram of a Linear InSb CID Focal Plane Array. The Output Video Waveforms Are Shown in the Inserted Photograph.

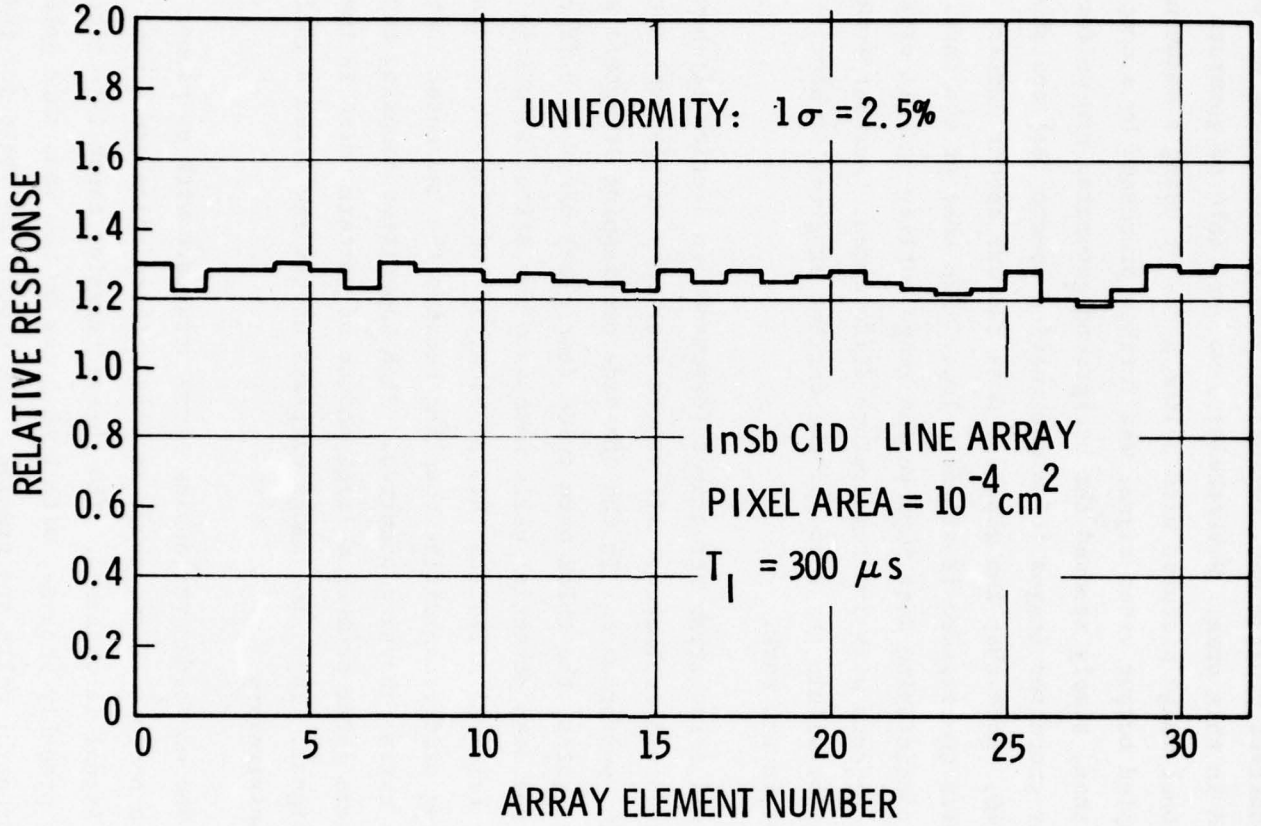


Figure 39. Variations in Relative Response of a 32-Element InSb CID Line Array.

for this particular array; better uniformity can be achieved with more effort. It should be pointed out that the line array work is not a part of the current program and, therefore, very little effort has been expended in this area. Nevertheless, we were able to generate two-dimensional image pictures with a line array by using a scanning mirror. The sampled output video signal was further processed by a computer, which, then, simply removed the background-generated non-uniformity. The computer processed images (of a man wearing spectacles) are shown in Figure 40. Note that the glasses, nose and ear appear darker, indicating that their temperature is slightly lower than that of the face. Here, signal conditioning does improve the image quality and did differentiate between objects with low temperature differences. Further work in this area is not within the scope of the current program; it should be considered for future work.

All three array structures (discussed in Section II) have been fabricated and evaluated. All showed that they do operate, but with quite different performance. In the one-side overlapping structure with parallel gates, the thick gate oxide (top gate) makes it difficult to create the deep potential wells necessary for effective charge transfer. When we tried to alleviate this problem, by reducing the thickness of the isolating oxide, capacitive coupling between the two gates increased and, in some cases, shorting occurred. High capacitive coupling between the row and column gates creates a large amount of pattern noise in the output video signal. Thus, the image displays of the raw video signals were less than satisfactory.

The one-side overlapping array structure with co-planar gates operates better. Here, there is less pattern noise and a more uniform output signal is obtained. The charge transfer capability also is much better, probably because, with both gates on the same thin gate oxide, deep potential wells are created. The processing yield for this structure is also better; we have found a half dozen operating arrays in one wafer, which we have not yet completely evaluated. The imaging results shown in Figures 34 - 37 were obtained from these arrays.

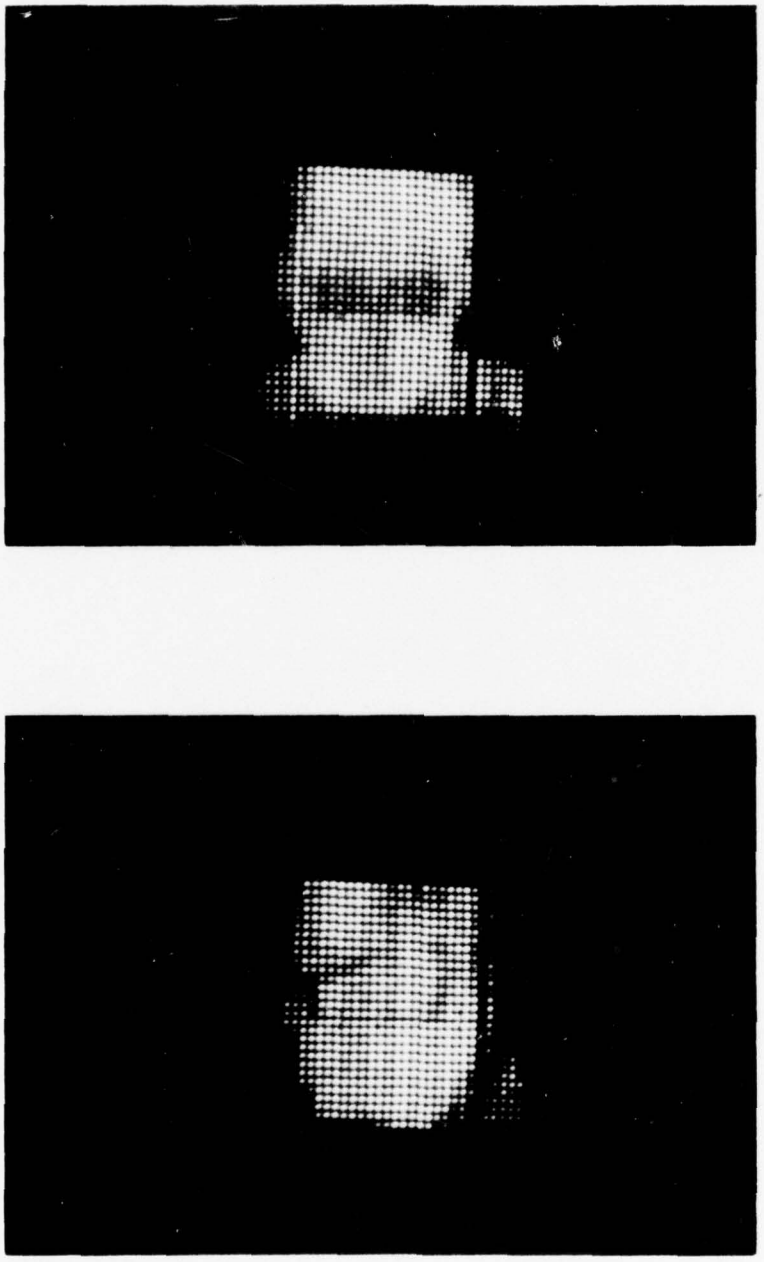


Figure 40. Image Pictures of a Man Wearing Glasses Obtained with a 32-Element InSb CID Line Array and a Computer Signal Conditioning.

The multi-side overlapping structure was also evaluated. Optical sensitivity is reduced in comparison with the other structures, probably because the gold metal layer used in the array structure obscures more of the sensing areas.

Based on these results, we feel that an even better array structure can be built, using a p-coupled scheme. Since both gates in the p-coupled structure can have the same thin gate oxide, deep potential wells can be created. Also, because the row and column gates in the p-coupled array are physically separated, capacitive coupling between them, and therefore pattern noise, is minimized. The operation of this array should be simpler because the row and column gates can have the same operating voltages.

SECTION VI. THEORETICAL ANALYSIS OF InSb CID ARRAY PERFORMANCE

1. Introduction

Because of the rapidly advancing state-of-the-art of InSb CID arrays, these devices are prime candidates for IR focal plane arrays, to be operational by the 1980's. As shown in the previous sections, we have successfully fabricated and demonstrated two-dimensional InSb CID arrays. Here, we present a theoretical analysis of such arrays to show their ultimate performance. Array performance is, of course, limited by the inherent noise sources associated with InSb CID arrays. All of these sources have been identified and modeled theoretically. The modelling results agree, quantitatively, with measurements obtained on actual line arrays.

Measurements on an InSb CID line array showed a background-limited performance to background levels as low as mid-10^{12} photons/sec-cm^2[1], a level that is significantly lower than those encountered in many terrestial applications, such as ground-to-ground, ground-to-air, air-to-air and air-to-ground infrared sensing. Because of this background-limited performance value, it is expected that the sensitivity of these arrays can be improved considerably, by an amount proportional to square root of the number of array elements. As the number of array elements increases, however, the array sensitivity is decreased due to an increase in line capacitance and bandwidth; thus the size of the array is determined by the background flux, the array noise, and the readout rate.

2. Transfer Characteristic

In order to calculate the number of noise carriers in a CID array, the transfer function, including the readout circuit, is required. The transfer characteristic relates the output signal to the input photon signal; it is often referred to as responsivity, with dimensions volts/watt or volts/photon. The overall transfer function can be divided into two parts; 1) the number of charge carriers per photon and 2) the output signal voltage per charge carrier. The first item is a function of the quantum efficiency; the second term depends on the input parameters of

the readout circuit.

As the MIS capacitor is biased into the deep depletion region, creating a space charge under the biased capacitor gate, incident photons generate electron-hole pairs, with the minority carrier holes (for n-type substrates) stored as a positively charged inversion layer at the insulator-semiconductor interface. This minority carrier charge, Q_g, is related to the incident photon flux density, Φ, by

$$\frac{dQ_g}{dt} = q\eta\Phi \ ,$$

where q is the electronic charge and η is the quantum efficiency. The total charge (per unit area) stored during the integration time, T_I, is simply the time integral of the incident photon flux,

$$Q_g = q\eta\Phi \, T_I,$$

where we assumed that η is constant with time. The surface inversion charge, Q_g, is generated in both the depletion region of the gate and in the neutral area outside of the gate. The minority carriers generated outside of the space charge region are collected via carrier diffusion, which is a function of the carrier lifetime. Since the minority carrier lifetime of InSb material is very short (see the Appendix), it is expected that the contribution of the carriers, generated in the undepleted area, to the inversion layer charge will be small. However, all of the minority carriers generated inside the space-charge region are swept into the surface and contribute to the inversion layer charge in the MIS structure. For InSb CID arrays, therefore, we assume that Q_g is generated entirely in the depletion regions under the MIS gate electrodes.

As the inversion charge increases, the depletion depth decreases and, accordingly, the carrier generation volume shrinks. Thus, the quantum efficiency, η, could vary with time. But, any such variation would depend on the degree of penetration (i.e. the absorption coefficient) of the incident photons and on the substrate doping level. For high energy photons (short wavelength region) which are absorbed mostly at the surface, the effect of depletion depth in the quantum efficiency should be minimal.

This is what we have observed for InSb CID's. Our measurements show that the output signal voltages do not vary much with substrate impurity levels for a photon flux of short wavelength region ($4.5\mu m$)[3]. On the other hand, for lower energy photons (long wavelength; total blackbody of $500^{o}K$), the signal variation with impurity level is quite pronounced, decreasing with increasing doping levels[3]. In most instances photons in the 3-5 μm region have high absorption coefficients[4] and, thus, are absorbed at the InSb surface; therefore, the quantum efficiency can be assumed to be constant.

The effective applied gate voltage, V_g, measured at the flatband condition is:

V_g = the voltage drop in oxide + the surface potential at the InSb surface

$$= \frac{Q_M}{C_o} + \frac{qN_D x^2}{2\epsilon},$$

where

Q_M = is the total charge density on the metal gate

C_o = is the gate oxide capacitance per unit area

N_D = is the concentration of donor impurities (we use n-type substrates)

x = is the depletion depth measured from the surface and

ϵ = is the permittivity of InSb.

The total charge density, Q_M, must be equal to that of the InSb surface; so

$$Q_M = Q_g + qN_D x,$$

where $qN_D x$ is the InSb space-charge density in the depletion region and Q_g is the inversion charge density generated by the incident photon flux, Φ. Recombining these equations, we obtain for x,

$$x = \frac{-qN_D + \sqrt{(qN_D)^2 + \frac{2qN_D C_o (C_o V_g - Q_g)}{\epsilon}}}{\frac{qN_D C_o}{\epsilon}}$$

When a gate voltage is applied, a deep depletion is instantaneously created, where the inversion charge, Q_g, is zero. This initial depletion depth, x_i, can be determined from the above equation by letting $Q_g = 0$. For InSb CID's, the following data are used to compute the value of x,

$$C_o = 3\times10^{-8}\ F/cm^2$$

$$\epsilon = 1.5\times10^{-12}\ F/cm$$

$$V_g = 2\ \text{volts.}$$

The calculated values of x_i for two doping levels are

$$x_i = 1.5\ \mu m \text{ for } N_D = 10^{15}\ cm^{-3},$$

$$x_i = 5.6\ \mu m \text{ for } N_D = 10^{14}\ cm^{-3}.$$

As the inversion charge, Q_g, builds up at the surface during the charge storage period, the depletion depth decreases; thus, the final value of the potential well depth, x_f, is a function of Q_g. For example, if

$$Q_g = \frac{C_o V_g}{2},$$

the inversion charge is approximately equal to half of the saturation charge ($\sim$ half full in the potential well). The final depletion depth, x_f, can also be computed for the two doping levels, as above,

$$\left.\begin{aligned} x_f &= 0.96\ \mu m \text{ for } N_D = 10^{15}\ cm^{-3} \\ x_f &= 3.86\ \mu m \text{ for } N_D = 10^{14}\ cm^{-3} \end{aligned}\right\} \ \&\ Q_g = C_o V_g/2$$

CID readout is achieved by simply removing the bias potential, thus injecting the stored charge. The injected charge appears as a displacement current on the line connected to the sensor. The net charge, Q_s, consists of two parts, the inversion layer charge, Q_g, and the net charge of the depletion region resulting from the gate voltage change (due to the injection pulse applied to the sensing line). When charge injection takes place, by removing the gate voltage, a number of majority carriers (equal to $Q_g + qN_Dx_f$) flow into the substrate to recombine with the minority carriers.

These majority carriers left the substrate during the charge storage period prior to injection. As the gate voltage is reapplied, after injection, a fresh depletion region is formed, allowing the number of majority carriers (equal to $qN_D x_i$) to leave the substrate. During the injection period, it is assumed that the minority carriers, charge Q_g, are completely neutralized by majority carriers. It can be shown (see Appendix) that, within a 50 ns injection period, a complete carrier recombination takes place in InSb CID's. Therefore, the net charge, Q_s, is equal to,

$$Q_s = Q_g + qN_D x_f - qN_D x_i$$

$$= Q_g - qN_D(x_i - x_f),$$

where the positive sign denotes the displacement current entering the substrate and the negative sign denotes charge leaving the substrate.

The output signal of the CID current is a result of the time integral of the displacement currents, which occur at the injection pulse; thus, the signal is directly proportional to the net charge, Q_s. Figure 41 shows the CID sequential readout circuit used to measure the signal voltage, which is a function of the total input capacitance, C_T. The signal voltage, V_s, is given by

$$V_s = \frac{Q_s A_d}{C_T},$$

where A_d is the sensor area and

$$C_T = C_I + C_{sh} + C_{col},$$

in which

C_I is the injection coupling capacitance,

C_{sh} is the total shunt capacitance of the sense line plus the effective input capacitance of the preamplifier transistor and

C_{col} is the total capacitance of the unselected elements in the column line.

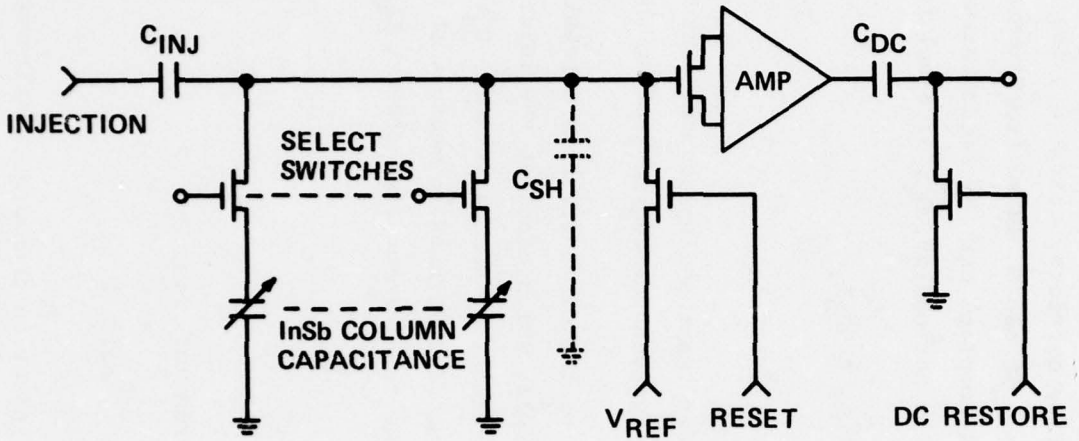


Figure 41. Equivalent Circuit of the Input Preamplifier for Enable-Line CID Readout Technique.

In terms of the input photon flux, Φ , the output signal can be now expressed as

$$V_s = \frac{\left\{q\eta\ \Phi\ T_I - qN_D\ (x_i - x_f)\right\}\ A_d}{C_I + C_{sh} + C_{col}} \quad .$$

As shown, the output signal is not a linear function of the photon flux because of the $x_i - x_f$ term, which is, in part, a nonlinear function of Φ. The nonlinear relationship between V_s and Φ , however, can be reduced by using a substrate with a low N_D value. Also, for small signal cases where $Q_g \ll C_o\ V_g$, the contribution of the nonlinear terms should be very small and, thus, the output signal is a linear function of the input photon flux. For high signal levels, where Q_g is near saturation, the nonlinear effect becomes important; in the example used above, if the inversion layer charge is half of the saturation, the decrease in signal charge is about 30% for $N_D = 10^{15}$ cm^{-3}, and for $N_D = 10^{14}$ cm^{-3} the reduction is only about 10%. Therefore, lightly doped substrate material is more ideal for CID applications.

For small signal level analysis, the overall transfer characteristic is given by,

$$R \simeq \frac{q\eta\ T_I\ A_d}{C_T} \qquad \text{Volts/photon/sec-cm}^2$$

$$\simeq \frac{q\eta}{C_T} \qquad \text{Volts/photon}$$

The transfer function of the output signal versus the input charge carriers is simply,

$$R_c \simeq \frac{q}{C_T} \ , \qquad \text{Volts/carrier}$$

From these transfer function equations, the noise equivalent carriers, $\overline{N}_{eq}$, (or NEC) can be determined, given the noise voltage, $\overline{V}_n$.

$$\overline{N}_{eq} = \frac{C_T}{q}\ \overline{V}_n$$

3. Noise Sources

a. KTC Noise

For CID readout, a reset switch (see Figure 41) is employed to bias the array sensor gates to a reference voltage, V_{REF}. Prior to every applied injection pulse, the reset switch is opened and the signal is read out. After sensing the signal voltage, the reset switch is reapplied to bias the sensing line. Due to the thermal noise in the channel of the reset transistor, the reset switch causes an uncertainty in the sense line voltage, resulting in KTC noise[5], the magnitude of which is,

$$\bar{V}_{nC} = \sqrt{kT/C_T},$$

where k is Boltzmann's constant and T is temperature. Thus, the noise equivalent carriers ($\bar{N}_{eq}$) is simply

$$\bar{N}_{eqC} = \sqrt{kTC_T}/q$$

As for the total input capacitance, C_T, the total capacitance (C_{col}) of unselected elements in the column line (the column that is connected to the sense line) is a function of the number of array resolution elements. As the number of array elements increases, C_{col} also increases and the array sensitivity is degraded. For 16x24 arrays, the column line (16-elements) capacitance is about 7 pF (this is a combination of oxide and depletion capacitance in the column line). The total shunt capacitance of a 32-stage, silicon shift register scanner sense line and the effective input capacitance of the preamplifier transistor (MOSFET) used with these arrays are approximately equal to 5 pF. If we use an injection-coupling capacitance of 3 pF, then the total system input capacitance, C_T, is equal to about 15 pF.

Using this capacitance value and a temperature, T = 77°K (since the reset switch operates at this temperature in the dewar), the KTC noise is approximately 800 carriers. As shown below, this is the largest source of noise in the system. This noise component, however, can be completely eliminated by using a correlated double sampling technique[6]. To do this, it is only necessary to measure the voltage difference before and after

charge injection using two sample pulses, the dc restore and the sample pulses. The dc restore pulse is applied after the reset switch is turned off, but before the injection, and sample pulse is applied after injection. Then the difference in voltage (signal voltage) between these two sample pulses is measured. This procedure cancels the KTC noise of the reset switch. Since the dc restore sampling is done after signal amplification, the contribution of its own KTC noise can be made small.

The use of a dc restore pulse, however, slows down array readout speed, since there must be three pulses for each element time - dc restore, injection and sample. For InSb CID arrays, the element time can be made as low as about 0.5 μs, since a complete injection takes place in less than 50 ns (see the Appendix). Thus, the operating frequency is 2 MHz, which is just about the upper limit for this readout method. For higher operating frequencies, other readout techniques are necessary.

b. Selection Switch Thermal Noise

As the column line is selected sequentially for signal readout, the turn-on resistance of the MOSFET selection switch is in the signal path and contributes to Johnson noise. The noise voltage generated by this resistance, R_{so}, is

$$\bar{V}'_{nR} = \sqrt{4kT\, R_{so} \Delta f} \quad .$$

where Δf is the amplifier bandwidth.

Since this noise voltage source is between the column capacitance, C_{col}, and the other two capacitances, it is divided between them. Thus, the noise voltage ($\bar{V}_{nR}$) appearing at the preamplifier input is

$$\bar{V}_{nR} = \frac{C_{col}}{C_T} \sqrt{4kT\, R_{so}\, \Delta f} \, ,$$

and thus the number of noise equivalent carriers is

$$\bar{N}_{eqR} = \frac{C_{col} \sqrt{4kT\, R_{so}\, \Delta f}}{q} \quad .$$

The turn-on resistance, R_{so}, is, typically, 10^3 ohms at 77°K, which yields a value of noise voltage of 10^{-9} volts/$\sqrt{Hz}$. In the above example, with a 2 MHz sampling rate, the amplifier bandwidth, Δf, should be approximately four times the Nyquist frequency; thus, $\Delta f = 4$ MHz. This is because the amplifier must be able to follow the settling time of the injection pulse in order for the signal voltage to be sampled. Therefore, the Johnson noise due to the turn-on resistance of the MOSFET switch, appearing at the input of the preamplifier, is 2×10^{-6} volts for a 4 MHz bandwidth. The noise-equivalent carriers of this noise voltage is then 180 carriers.

The distributed resistance of the sensing column line also contributes Johnson noise to the system, if it is significant, compared with the turn-on resistance. Our array processing allows us to use a high conductivity metal bus line to minimize column resistance. Thus, we can assume that the Johnson noise generated by column conductor resistance is negligible.

c. Amplifier Noise

We use a preamplifier (p-channel, MOSFET) inside the dewar, as an on-chip amplifier. The first stage of the amplifier should be integrated as closely as possible to the column sense line to minimize the input capacitance to the transistor gate. In this case, the first stage amplifier is operated at the same temperature as the InSb CID, 77°K, which reduces the Johnson noise.

The amplifier noise voltage from the MOSFET channel resistance is

$$\bar{V}_{ng_m} = \sqrt{\frac{8}{3} kT \left(\frac{1}{g_m}\right) \Delta f},$$

where g_m is the transconductance of the MOSFET, and is related to the device dimensions and the mobility value at 77°K. The transconductance of the MOSFET device used for these arrays is about 5000 μmhos at a drain current of 2 ma. For a 4 MHz bandwidth, the amplifier noise voltage is equal to 1.5×10^{-6} volts and, thus, the corresponding number of noise equivalent carriers, $\bar{N}_{eq}$ for 16x24 arrays, is about 140.

In addition to the Johnson noise of the amplifier, for physically realizable MOSFET's, the transistor exhibits a relatively large amount of 1/f noise which must be included in the amplifier noise computation. The noise spectral power density of the MOSFET is,

$$E_n^2 (f) = \frac{8\ kT}{3\ g_m} + \frac{7x10^{-9}}{f^2} \quad ,$$

where the second term represents the spectral density of 1/f noise. Since the reset and dc restore switches are periodically closed at the element rate, after sampling the signal of each element, the system acts like a bandpass filter for noise, suppressing the low-frequency noise. The effective low cutoff frequency is the sampling rate, f_s, and the upper cutoff frequency is determined by the required bandwidth; $\Delta f = 2f_s$. Thus, the noise content in this bandpass can easily be calculated by integrating the power density from f_s to $3f_s$. Then, the noise voltage is

$$\bar{V}_{nA} = \sqrt{\frac{8\ kT\ \Delta f}{3\ g_m} + \frac{7x10^{-9}x4}{3\ \Delta f}} \quad ,$$

where $\Delta f = 3f_s - f_s = 2f_s$.

For high-frequency operation, therefore, the 1/f noise contribution is small and the dominant amplifier noise is the Johnson noise. For the above example, the 1/f noise term is very small, only about $5x10^{-8}$ volts; the amplifier Johnson noise is $1.5x10^{-6}$ volts. As the sampling frequency decreases, however, the contribution of 1/f noise voltage increases significantly, and it could become dominant.

An improvement in the 1/f noise of the preamplifier transistor can be made by using JFET's rather than MOSFET's, since 1/f noise is associated with interface states. This is a subject for future study.

d. Dark Current Shot Noise

We have assumed, up to now, that the inversion charge density, Q_g, is generated by the incident photon flux only. However, thermally generated minority carriers can also be collected and stored as inversion

charge. Thus, Q_g can consist of the minority carriers generated by the incident photons and thermally generated minority carriers. The inversion charge density from thermal generation yields an output signal voltage that is constant with time and can be removed from the true signal. However, the shot noise due to the thermally generated dark current, cannot be removed; thus system sensitivity is limited.

In order to compute the dark current shot noise, we need a correct model of dark current generation. Our earlier experimental work on InSb MIS structures strongly suggests that the dark current is dominated by thermal bulk generation process in the depletion region under the MIS capacitor gates[4]. The dark current, thus, is a function of the depletion depth which is, in turn, a function of time. A detailed derivation of the dark current is given in our IRIS paper[7]; only the results are presented here.

Figure 42 shows the integrated dark current carrier density plotted as a function of storage time (which was calculated from the model). The saturation characteristic of this curve has been confirmed by experiment[8,9]. The capacitance-time (C-t) measurement indicates that the MIS capacitance thermal relaxation time is in the order of 0.3 seconds at $77^{o}K$. The maximum storage charge in the MIS capacitor was also checked using an IR saturation measurement. The saturation carrier density was about $2x10^{11}$ carriers/cm^2 The dot points shown in Figure 42 were obtained from dark current noise measurements of a line array, as shown in Figure 43 . Here, the integration time, T_I, was varied by changing the input clock frequency of the silicon shift-register scanner; thus, at each data point, we measured the system noise, without the dark current noise component, and the total noise, including the dark current. Then, we determined the dark current noise voltage. From the responsivity data we were then able to find the number of rms noise carriers associated with the integrated dark current. As shown in Figure 43 the number of rms noise carriers depends on the square root of the integration time, indicating that it is shot noise in nature. Therefore, the number of integrated dark current carriers is equal to the square of this noise value at a given integration time. The resultant integrated dark current

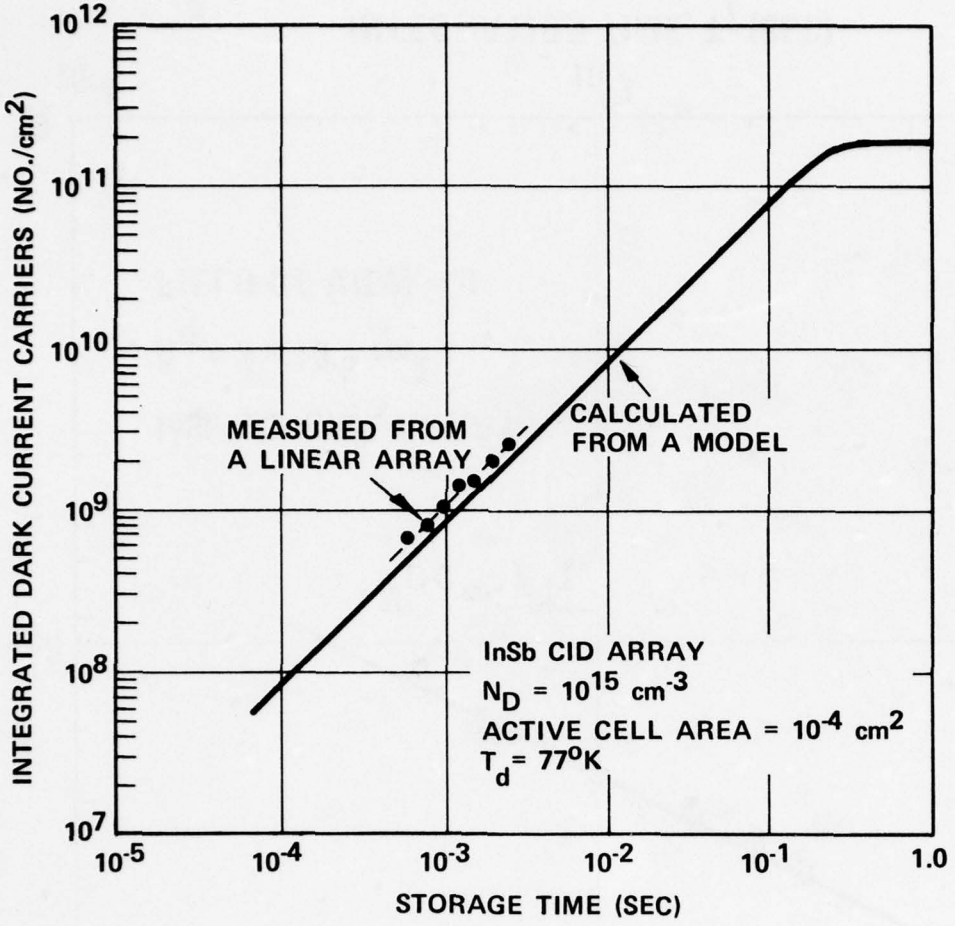


Figure 42. Thermally Generated Dark Current Carrier Density Versus Storage Time for N-Type InSb Materials.

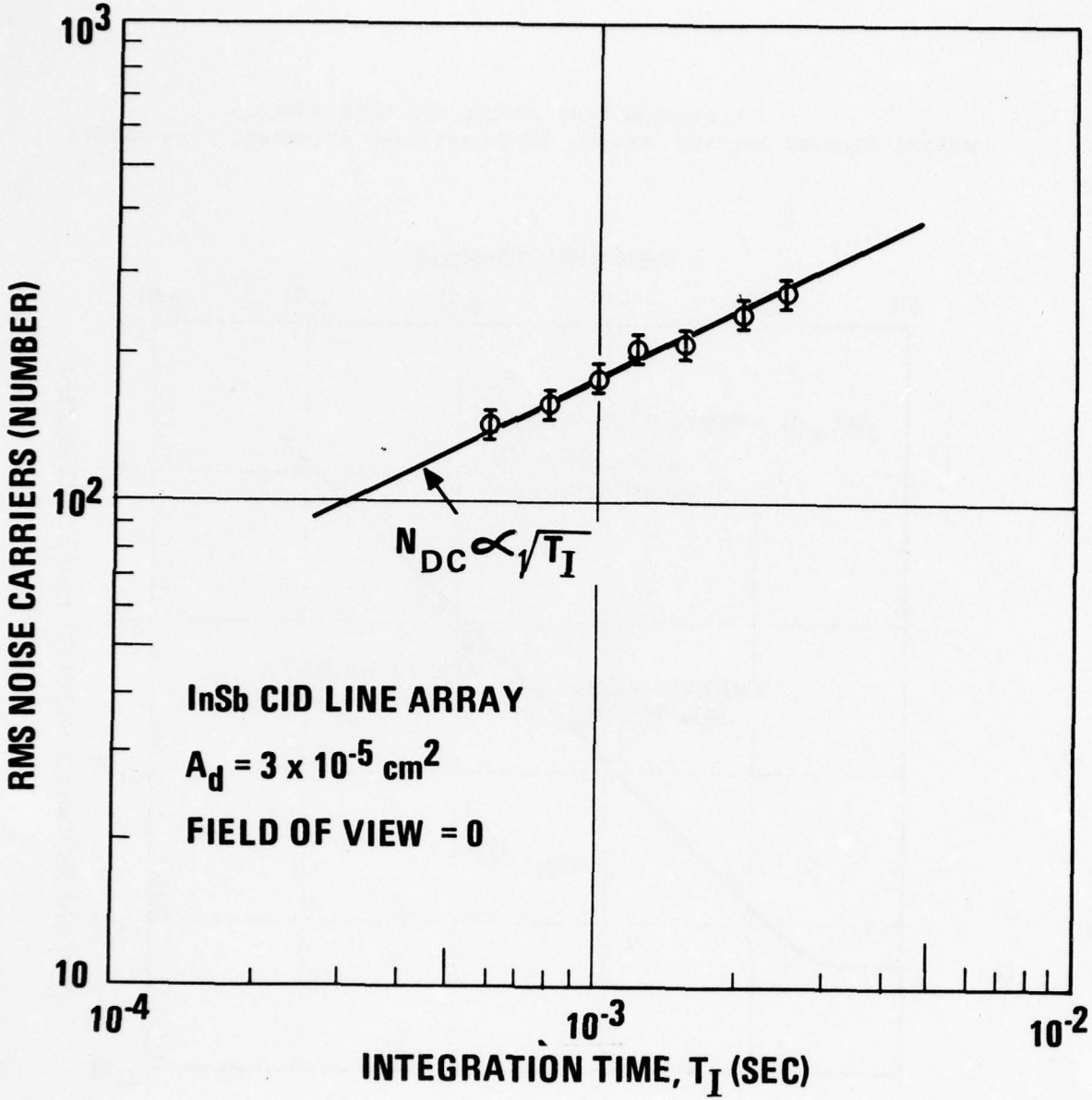


Figure 43. Measured RMS Noise Carriers Associated with the Integrated Dark Current Versus Integration Time.

carriers are shown, and compared with the calculated model, in Figure 42

The dark current carrier generation rate per unit area is 8×10^{11} carriers/sec-cm^2, which corresponds to a current density of 0.13 $\mu a/cm^2$. This value of current density is well within the value obtained using typical InSb p-n junction diodes. The number of dark current carriers, N_{DC}, is

$$N_{DC} = 8 \times 10^{11} A_d T_I .$$

The number of rms noise carriers, due to the integrated dark current, is,

$$\bar{N}_{eqD} = \sqrt{N_{DC}}.$$

The relationship between sampling frequency and integration time is,

$$f_s = \frac{n}{T_I} ,$$

where n is the total number of array resolution elements. Again, for a 2 MHz sampling rate and a 16x24 array ($n \simeq 400$), the required integration time is about 200 μs. The active area of each pixel in this array is 2.58×10^{-5} cm^2 (2x2 mils element size). Under these conditions, $N_{DC} = 4000$ carriers and, thus, $\bar{N}_{eqD} = 63$ carriers. It is interesting to note that, in this example, the amount of integrated dark current shot noise is much less than the other noise sources discussed above.

e. Photon Shot Noise

Since InSb CID arrays are designed as photon counters or photon sensors, the photon shot noise contribution must be considered. In IR systems, there are two types of photon fluxes that the array sees; these are (1) the background photon flux radiated from the dewar window, array front optics, etc., and (2) the signal photon flux generated by a small temperature difference in the scene. In most applications, the background photon flux is much greater than the signal photon flux. If the sensitivity of an IR sensor system is limited by the background component, it

is termed a background-limited performance (BLIP) device which is the best device attainable . Because of the high photon shot noise levels encountered in IR sensor systems, the other noise components are usually less dominant; thus, InSb CID arrays can become ideal IR sensor systems. The study of these array noise sources enables us to tailor the design of arrays for particular applications to achieve a BLIP operation.

The inversion layer charge stored in the MIS interface also consists of charge generated by the relatively large amount of background photon flux, which, in turn, enhances array saturation. Accordingly, the maximum integration time depends on the background photon flux levels, as shown in Figure 44.[7] Here, the maximum integration time is plotted as a function of the incident photon flux at three different operating temperatures. The analysis uses the dark current generation model discussed previously. As shown, at $77^{o}K$, the maximum storage time tends to saturate a background photon flux level of about mid-10^{12} photons/sec-cm^2. This is due to dark current generation and, in low background regions, the number of integrated dark current carriers controls this saturation. At lower temperatures, however, the maximum integration time increases at lower background levels, as expected.

The number of carriers generation (N_B) by the background photon flux, Φ_B, is

$$N_B = \eta \Phi_B A_d T_I \ .$$

The background shot noise, $\bar{N}_{eqB}$, is the rms fluctuation in N_B and is equal to

$$\bar{N}_{eqB} = \sqrt{N_B} \ .$$

Typical background levels encountered in terrestial applications are in the range of 10^{14} photons/sec-cm^2. Using the above example, then, N_B is about 2.5×10^5 carriers for $\eta = .5$ and thus, the background shot noise, is 500 carriers. The dominant noise source in the InSb CID array sensor system for the above example is background photon shot noise, and,

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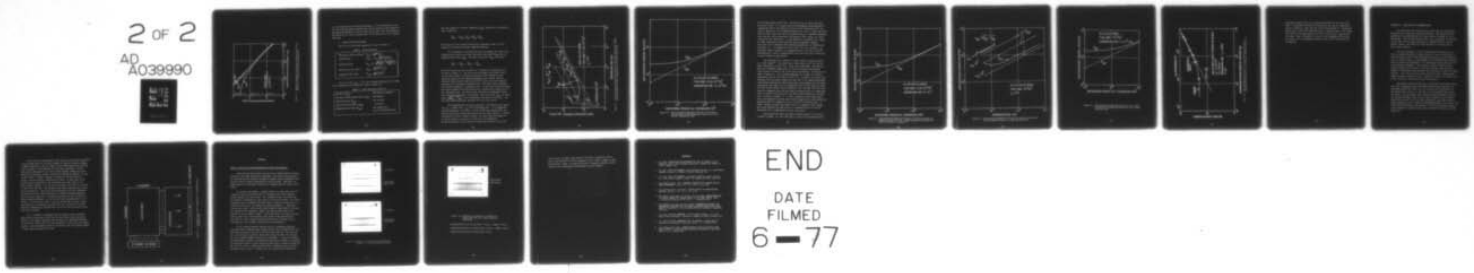

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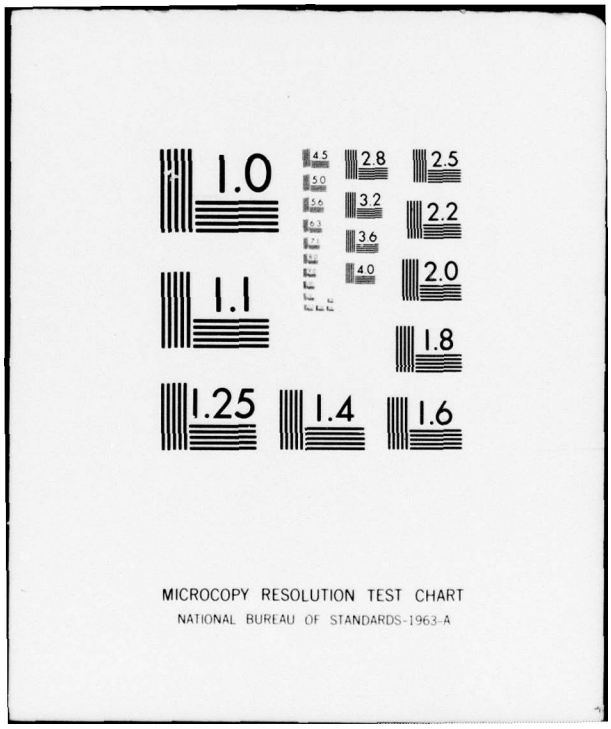
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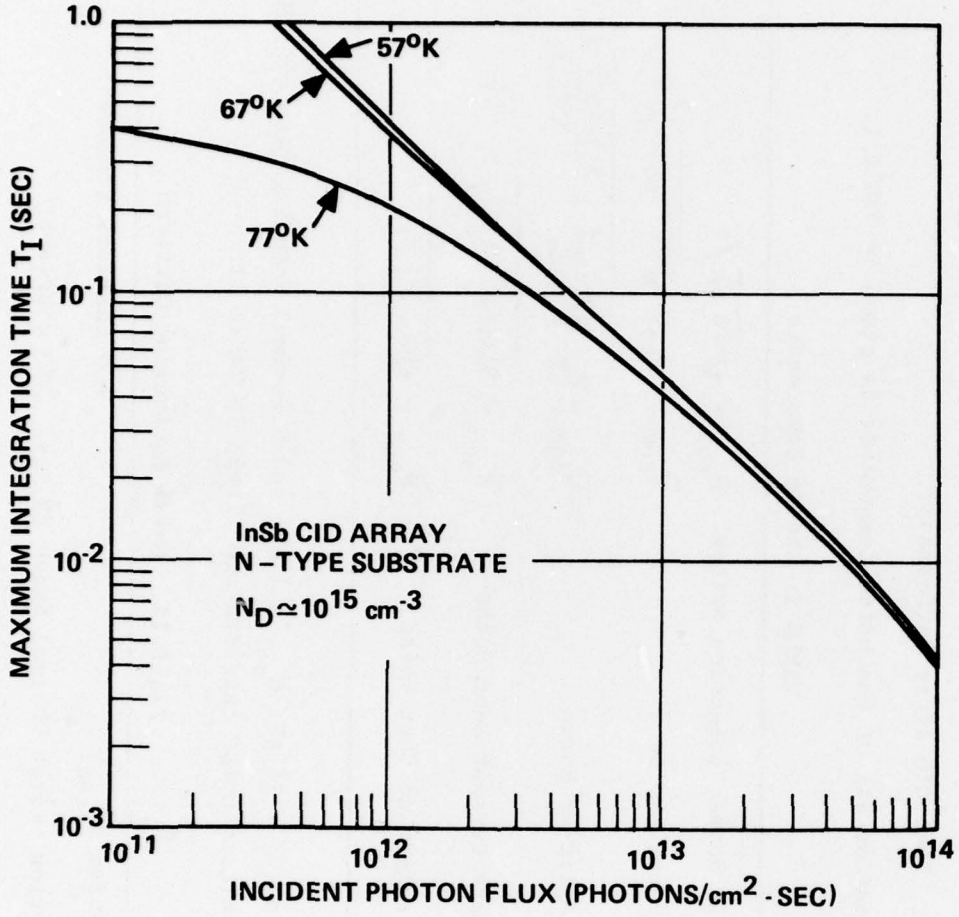


Figure 44. Maximum Integration Time Versus Incident Photon Flux Density for Different Operating Temperatures.

so, the system should yield BLIP performnace. It is interesting to note that the selection switch thermal noise and the amplifier noise depend on the amplifier bandwidth, while the dark current shot noise and background shot noise do not, but are proportional to the square root of the integration time.

4. InSb CID Array Performance

List of all of the noise components is given in Table I.

TABLE I: Noise Components

KTC Noise, Selection Switch	$\bar{N}_{eqC} = \sqrt{kTG\ C_T}/q$
Thermal Noise	$\bar{N}_{eqR} = C_{col}\sqrt{4kT\ R_{so}\Delta f}/q$
Amplifier Noise	$\bar{N}_{eqA} = C_T\sqrt{\frac{8kT\ \Delta f}{3g_m} + \frac{2.8\times10^{-8}}{3\Delta f}}/q$
Dark Current Shot Noise	$\bar{N}_{eqD} = \sqrt{8\times10^{11}\ A_d\ T_I}$
Background Shot Noise	$\bar{N}_{eqB} = \sqrt{\eta\Phi_B\ A_d\ T_I}$

For C_T = 15 pF, C_{col} = 7 pF, and a maximum sampling rate of 2 MHz, the calculated noise carriers are listed in Table II.

TABLE II. Noise Equivalent Carriers

KTC Noise ($\bar{N}_{eqC}$)	800 carriers (removed)
Selection Switch Thermal Noise ($\bar{N}_{eqR}$)	180 carriers
Amplifier Noise ($\bar{N}_{eqA}$)	140 carriers
Dark Current Shot Noise ($\bar{N}_{eqD}$)	63 carriers
Background Shot Noise ($\bar{N}_{eqB}$)	500 carriers for $\Phi_B = 10^{14}$ photons/sec-cm^2

The total number of all noise components ($\bar{N}_{eqT}$) referred to the amplifier input is given by

$$\bar{N}^2_{eqT} = \bar{N}^2_{eqR} + \bar{N}^2_{eqA} + \bar{N}^2_{eqD} + \bar{N}^2_{eqB} \quad .$$

Note that we did not include the KTC noise component, since it can be removed by the correlated double sampling technique.

It is convenient to describe CID array performance in terms of two combined noise sources, the total CID array system noise ($\bar{N}_{eqS}$) and the background shot noise, $\bar{N}_{eqB}$. The total array noise, $\bar{N}_{eqS}$, is simply,

$$\bar{N}^2_{eqS} = \bar{N}^2_{eqR} + \bar{N}^2_{eqA} + \bar{N}^2_{eqD} \quad .$$

The total array noise can be plotted as a function of integration time, as shown in Figure 45. The solid curve represents this noise source. In the valley region, total noise decreases as the integration time increases because of the bandwidth-dependent noise sources, such as selection switch thermal noise and amplifier noise, for which bandwidth decreases with increasing integration time. The noise, then, increases with further increases in integration time. In this case, the dark current shot noise dominates the total array noise, varying as the square root of the integration time. The dotted lines represent the background photon shot noise for given photon flux density. The total noise, $\bar{N}_{eqT}$, is simply equal to $\sqrt{\bar{N}^2_{eqS} + \bar{N}^2_{eqB}}$ at any integration time and for a given Φ_B. But the larger term practically dominates the total noise source.

The background shot noise is, basically, the dominant noise source for Φ_B, greater than $\Phi_B = 10^{13}$ photons/sec-cm^2; it is background-limited performance. Therefore, for most terrestrial applications, the InSb CID arrays are photon noise limited and are ideal systems. A further illustration of this is shown in Figure 46, where the total number of all noise sources is plotted as a function of the background photon flux density for the shortest integration time that can be used

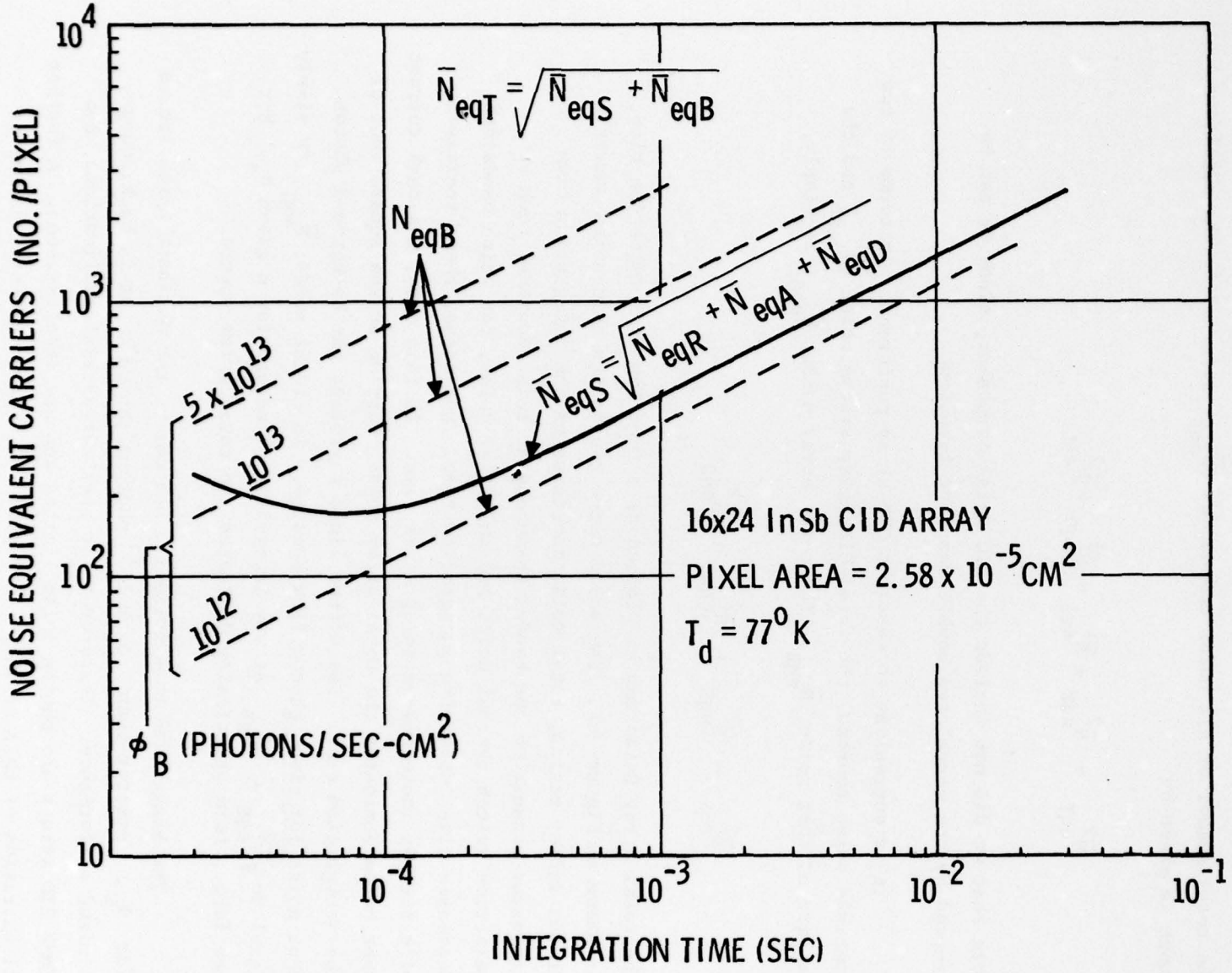


Figure 45. Calculated Noise Equivalent Carriers of the Total Array Noise ($\bar{N}_{eqS}$) Versus Integration Time, Comparing with Different BLIP Lines.

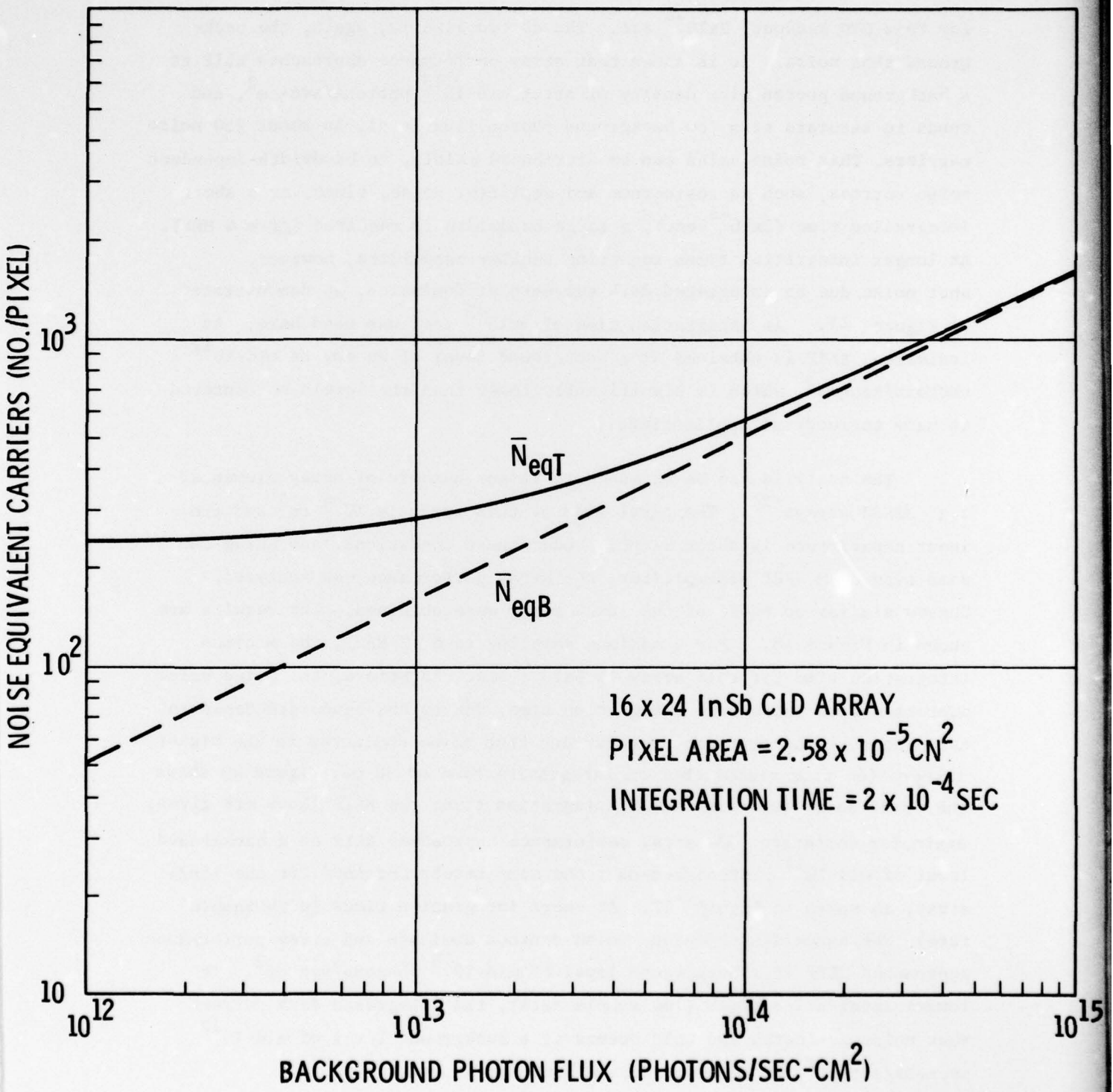


Figure 46. Calculated Noise Equivalent Carriers of All Noise Sources ($\bar{N}_{eqT}$) Versus Background Photon Flux for the Shortest Integration Time.

for this CID readout, $2x10^{-4}$ sec. The dotted line is, again, the background shot noise. It is shown that array performance approaches BLIP at a background photon flux density of about mid-10^{13} photons/sec-cm^2, and tends to saturate at a low background photon flux level, to about 250 noise carriers. This noise value can be attributed mainly, to bandwidth-dependent noise sources, such as resistance and amplifier noise, since, at a short integration time ($2x10^{-4}$sec.), a large bandwidth is required (Δf = 4 MHz). At longer integration times requiring smaller bandwidths, however, shot noise, due to integrated dark currents, predominates, as demonstrated in Figure 47. An integration time of $5x10^{-3}$ sec. was used here. As indicated, BLIP is obtained at a background level of as low as mid-10^{12} photons/sec-cm^2, which is significantly lower than the levels encountered in many terrestrial applications.

The analysis can be extended to larger numbers of array elements, e.g. 32x32 arrays[2]. The pixel area of this array is 10^{-4} cm^2 and the input capacitance is about 32 pF. Under these conditions, and using the same type of MOSFET preamplifier, the array performance was analyzed. Curves similar to those of the 16x24 array were obtained. The results are shown in Figure 48. For a maximum sampling rate (2 MHz), the minimum integration time for this array is $5x10^{-4}$ sec. As before, the noise value decreases with increasing integration time, due to the bandwidth-dependent noise sources and then the dark current shot noise dominates in the higher integration time region. For an integration time of 30 ms, Figure 49 shows the total noise carriers versus integration time; the BLIP lines are given, again, for comparison. The array performance approaches BLIP at a background level of mid-10^{12} photons/sec-cm^2, the same result obtained for the 16x24 array, as shown in Figure 47. At short integration times (high sample rate), the bandwidth dependent noise sources dominate and array performance approaches BLIP at a background level of mid-10^{13} photons/sec-cm^2. At longer integration times (low sample rate), the integrated dark current shot noise dominates and BLIP occurs at a background level of mid-10^{12} photons/sec-cm^2, as demonstrated in both array cases.

This analysis has been confirmed by measured data on line arrays, as shown in Figure 50. The solid line is a plot of the calculated noise

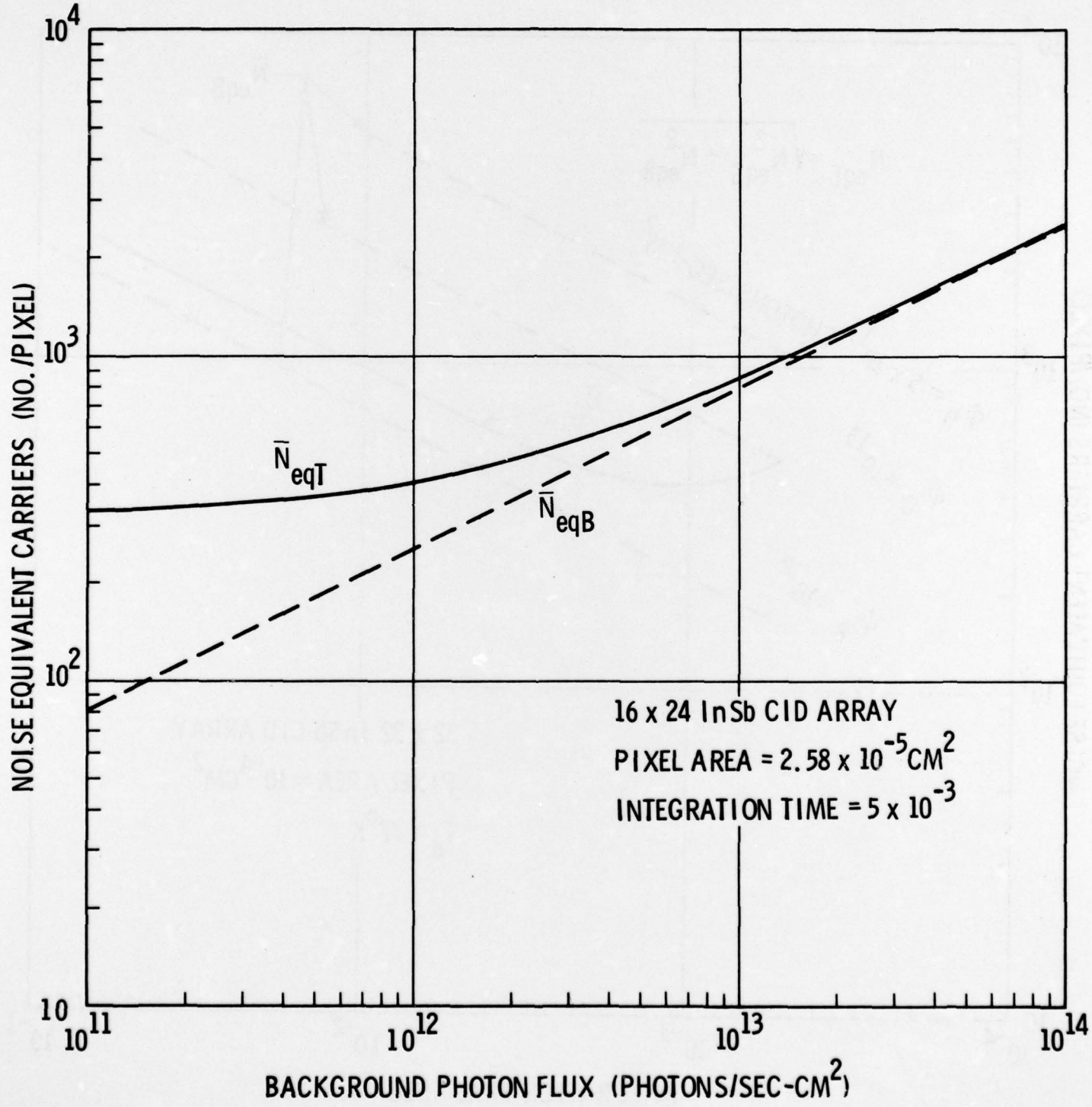


Figure 47. Calculated Noise Equivalent Carriers of All Noise Sources VS Background Photon Flux for a Longer Integration Time Than That Used in the Result of Figure 46.

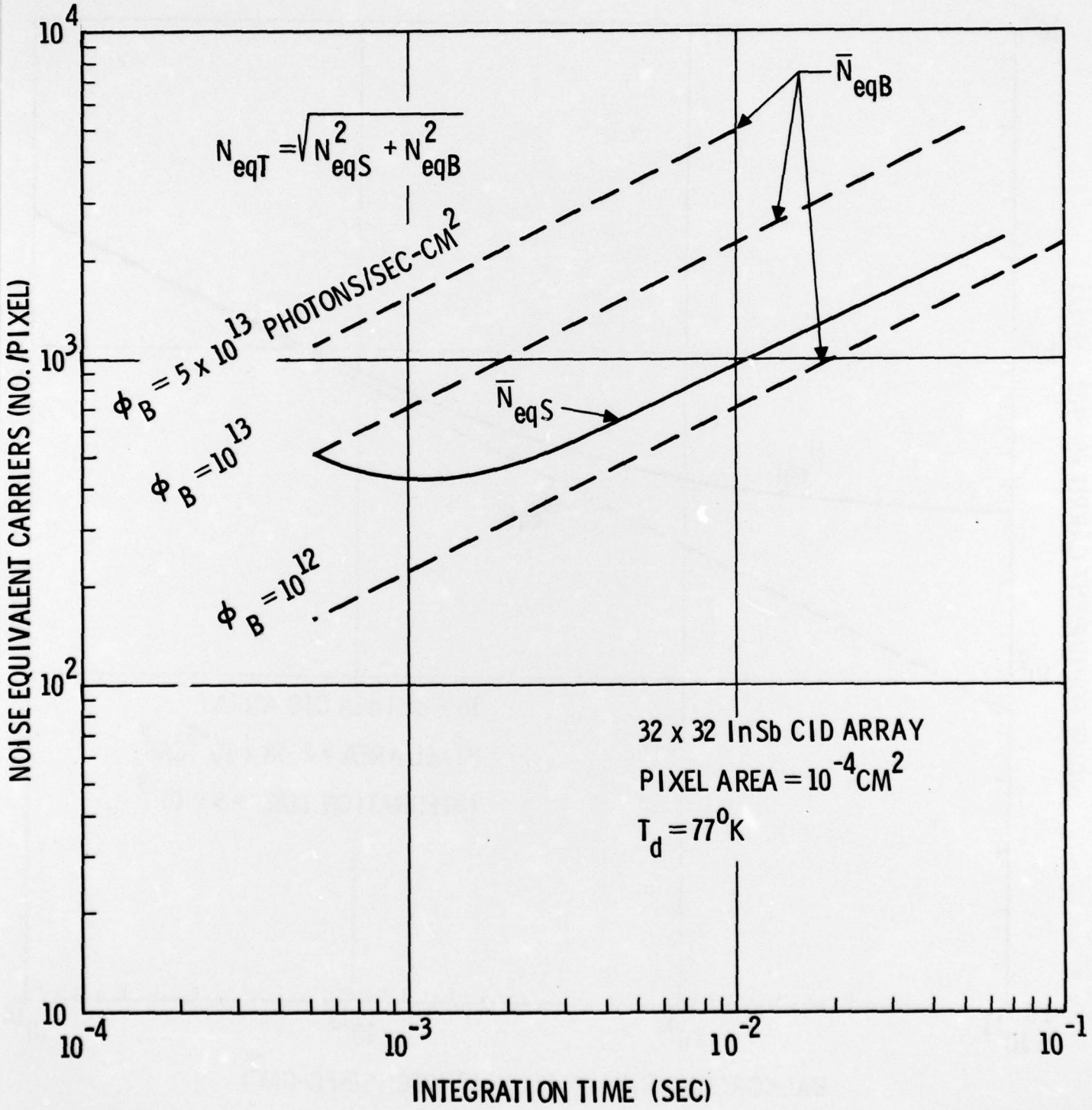


Figure 48. Calculated Noise Equivalent Carriers of the Total Array Noise Versus Integration Time for a 32x32 InSb CID Array.

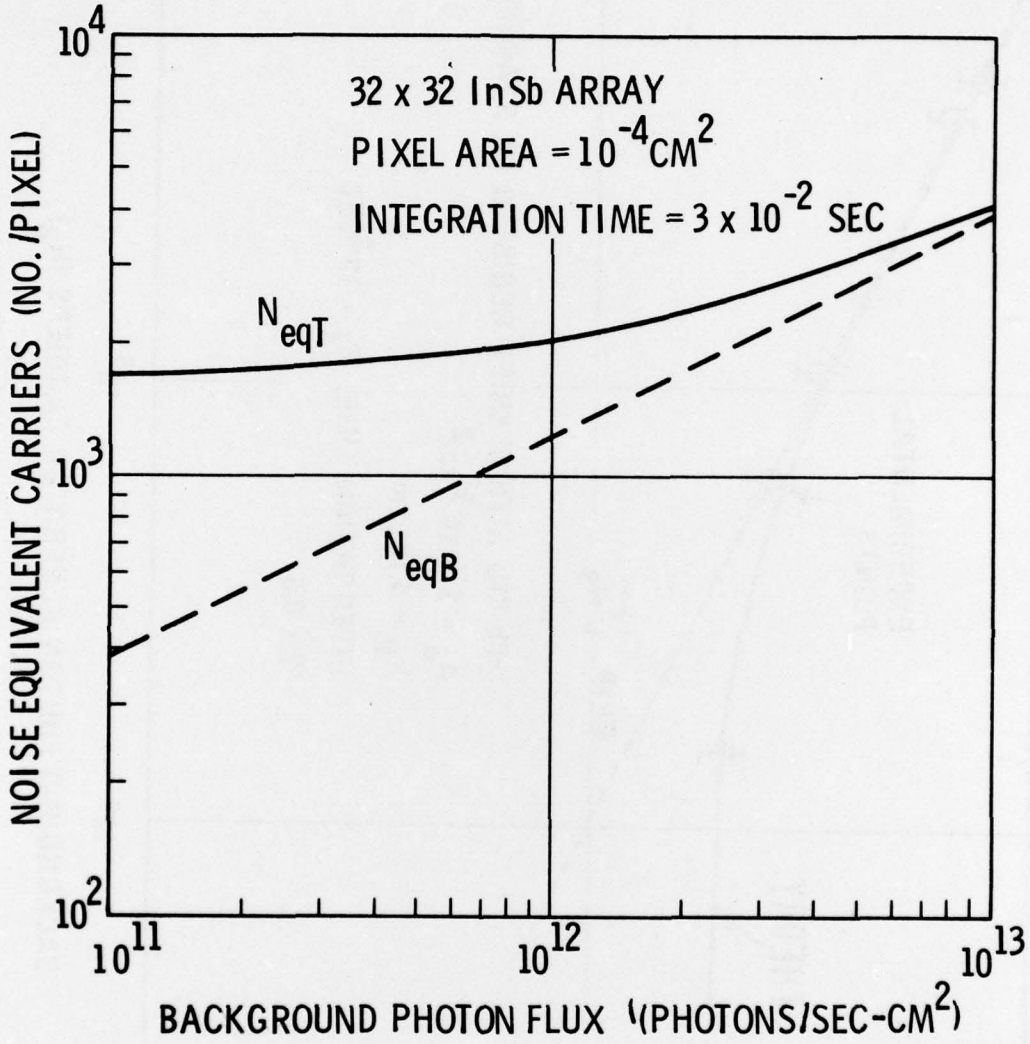


Figure 49. Calculated Noise Equivalent Carriers of All Noise Sources Versus Background Photon Flux for a 32x32 InSb CID Array.

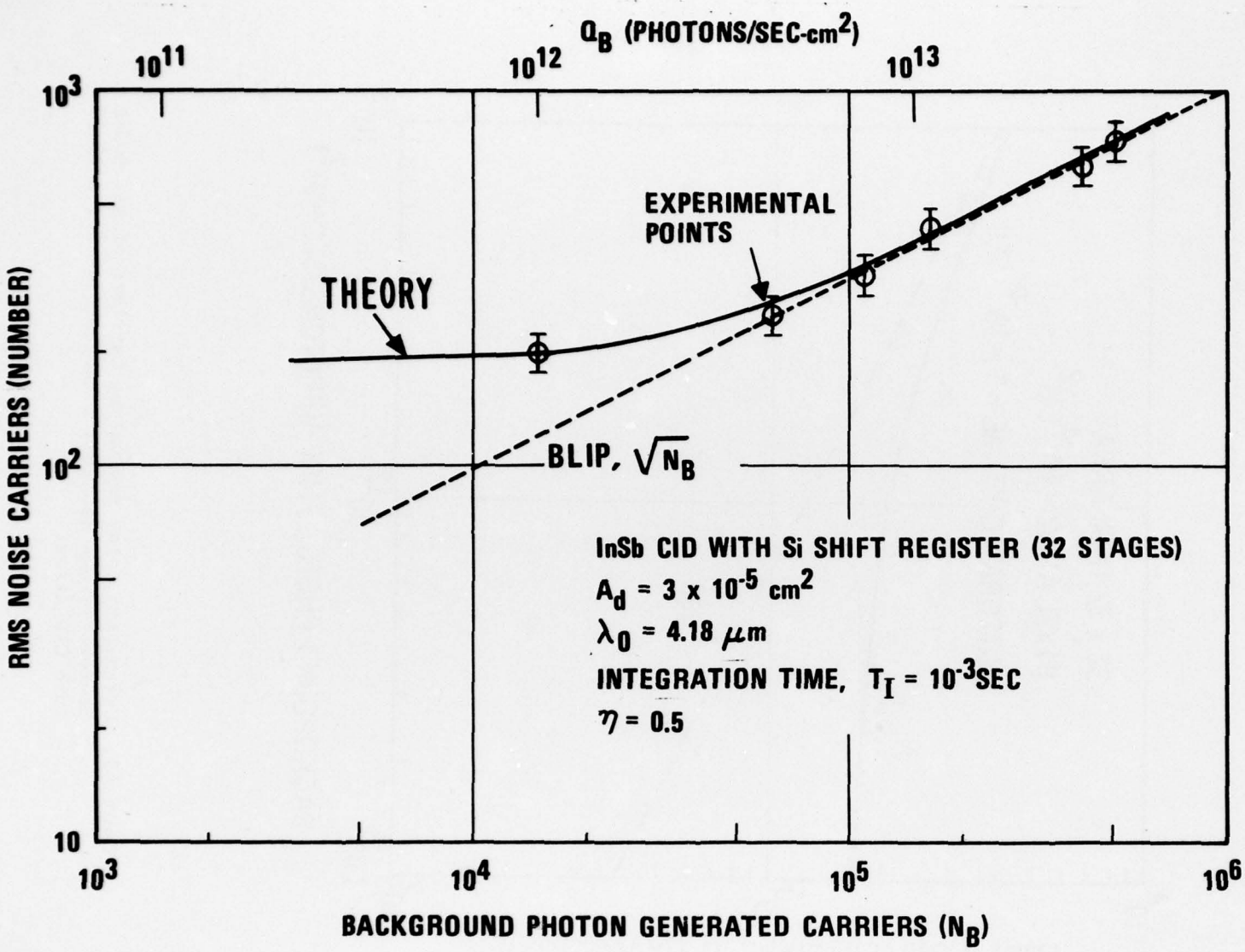


Figure 50. Measured RMS Noise Carriers of All Noise Sources Versus Background Photon Flux for a 32-Element InSb CID Line Array.

equivalent carrier values of all noise sources based on the array noise model. The agreement between the theoretical curve and the experimental points is excellent. Note that the results approach BLIP at a background photon level of mid-10^{12} photons/sec-cm^2, as indicated above. The integration time for this measurement was 10^{-3} sec, which gives a sampling rate of 32 KHz. Thus, performance is limited by the integrated dark current shot noise in the low background region, below mid-10^{12} photons/sec-cm^2, as expected.

SECTION VII. CONCLUSIONS AND RECOMMENDATIONS

Two-dimensional 16x24 InSb CID area arrays have been successfully fabricated via a multilayer processing technique. The arrays have been demonstrated by displaying real time raster-scanned IR images on an X-Y CRT monitor. These two-dimensional arrays will, eventually, be used with silicon CCD's for TDI signal processing in scanning systems. For the present, however, the arrays are being evaluated in a staring mode to verify their operation.

The main requirement in any two-dimensional CID structure is to obtain a complete transfer of charge between the row and column gates in each resolution element. Charge coupling between gates in each element, in order to transfer charge, is accomplished via an overlapped gate structure, three of which were investigated. All demonstrated array operation, but with differing performance. The co-planar structure turned out best, probably because with two gates on the same thin gate oxide, both are capable of creating the deep potential wells necessary for effective charge transfer. Also, there was less pattern noise and a more uniform output signal from these co-planar arrays. Patterns of "shapes" and "words" were clearly imaged on a CRT monitor using this structure.

Theoretical analysis showed that at low sample rates (long integration time), background limited performance (BLIP) can be obtained at a background photon flux level of as low as the mid-10^{12} photons/sec-cm^2. The dominant noise source, in this case, is the integrated dark current shot noise. For high sample rates, requiring large bandwidths, however, the bandwidth-dependent noise sources, such as amplifier and selection switch thermal noise, limit the array performance; thus, BLIP occurs at higher background levels. Among the bandwidth-dependent noise sources, the selection switch thermal noise dominates. This noise component, however, can be completely eliminated using a new InSb CID-Si CCD focal plane configuration.

In the earlier series-parallel scan, IR focal plane array concept[10], it was proposed that all the array elements be read out in series through a common preamplifier; then the signal would be demultiplexed and inserted into 24 parallel Si CCD registers for TDI signal processing. In this focal plane configuration, two silicon shift register scanners are still required for sequential readout (vertical and horizontal scanners, as used in this report). However, instead of reading out the whole array in series, a parallel readout technique can be used. In this case, all 24 column lines are connected to the Si CCD TDI chip rather than to a Si shift register scanner, as in the earlier approach, and read out in parallel into the Si CCD chip. The proposed focal plane configuration is illustrated in Figure 51. This focal plane configuration not only eliminates the selection switch, which contributes to dominant bandwidth-dependent noise, but also allows for a low sample rate which, in turn, reduces the required system bandwidth. As far as the hybrid interconnection is concerned, it is the same as before. The only penalty here is that 24 separate amplifiers are needed for parallel read out. But this is a simple amplifier configuration, although they must be low noise, and can be built into the Si CCD chip.

It is, therefore, recommedned that an attempt be made to combine InSb CID area arrays and Si CCD's for TDI focal plane array development. Because of the rapidly advancing state-of-the-art of InSb CID development, it is felt that these arrays are prime candidates for IR focal plane sensor systems. Array development should be continued to meet the expected demand of large system applications by 1980.

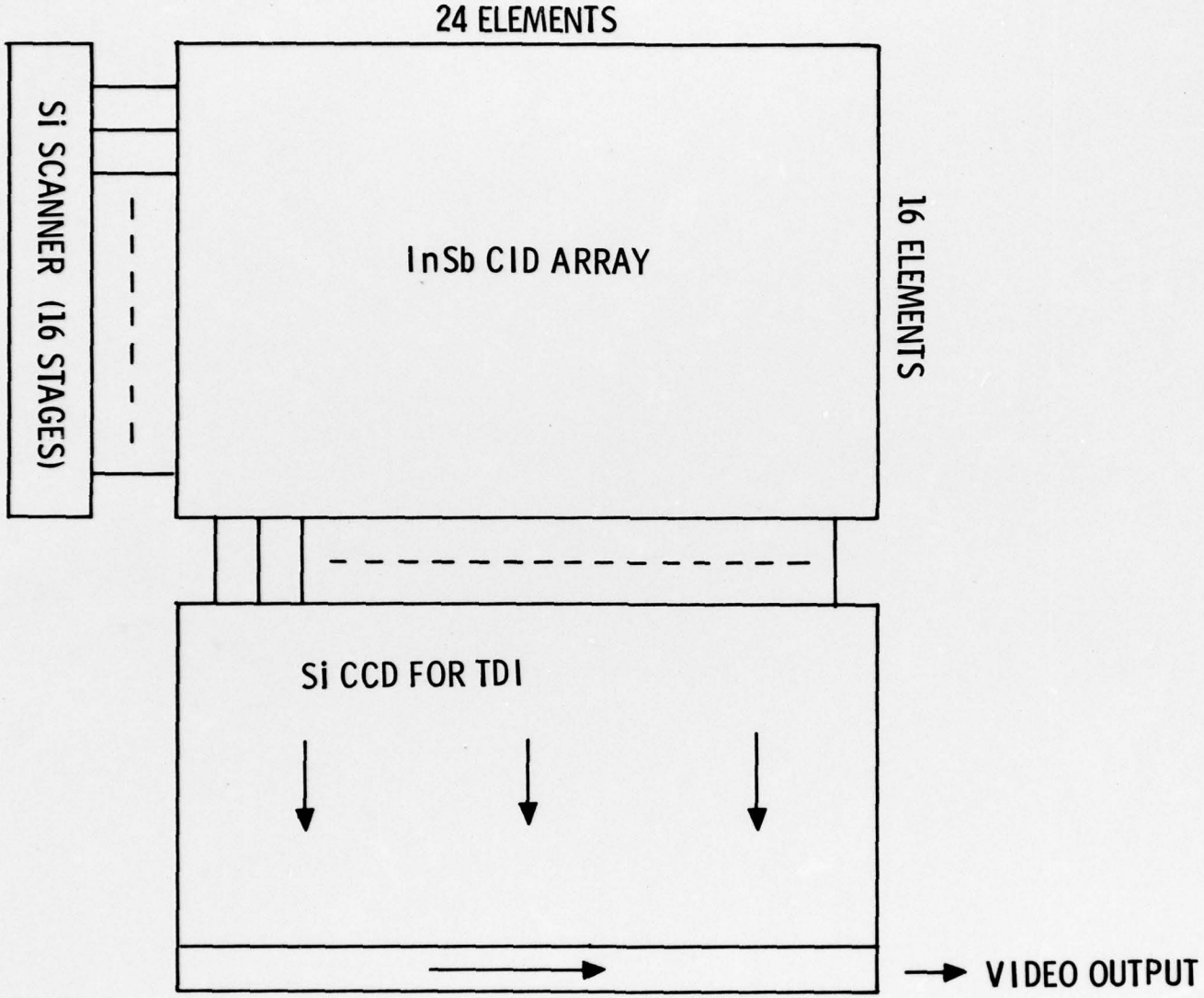


Figure 51. Proposed Focal Plane Configuration of InSb CID Array - Si CCD for TDI.

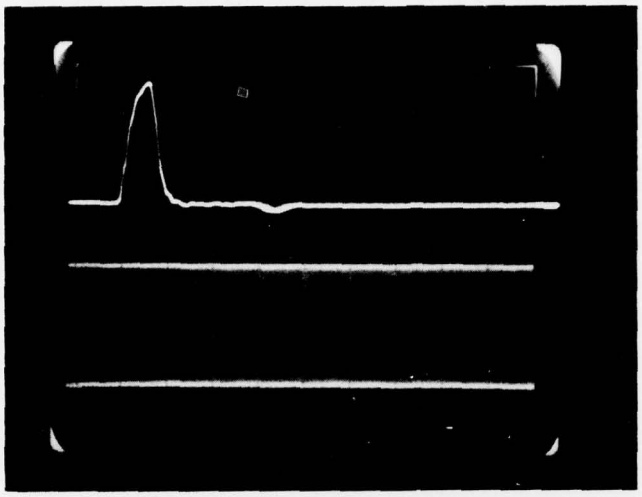
APPENDIX

Effect of Minority Carrier Recombination on InSb CID Operation

There has been some concern over the rate at which injected minority carriers in the InSb CID would be recombined. For proper array operation, the injected minority carriers (information charge) must be recombined with majority carriers before reapplying the injection pulse. Otherwise, the charge might be recollected, resulting in a lagging effect on signal information.

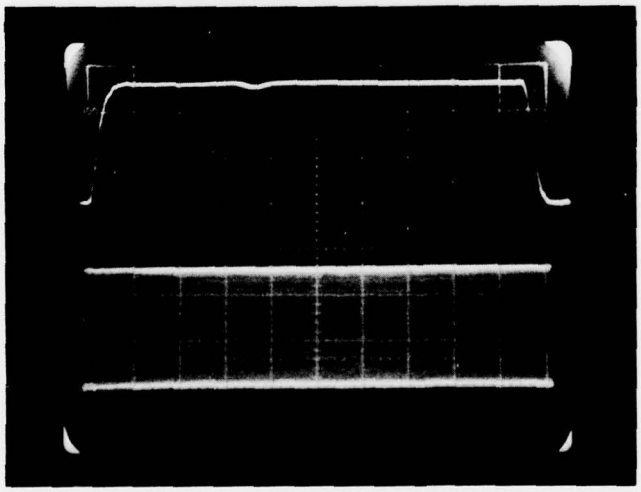
To evaluate this effect, a single element in a line array (4x4 mils resolution size) was monitored while a 32-stage silicon shift register scanner operated the entire array. The integration time of the InSb CID was adjusted by changing the input clock to the silicon scanner. At a given integration time, we measured the CID output ac signal as a function of the injection pulse width. The results are shown in Figure 52 . Each photo contains two traces: the top trace shows injection pulse width, the bottom one represents the modulated ac signal (the peak-to-peak value of the envelope is the ac signal voltage). In the top photo, the injection pulse width is about 50 ns; the injection pulse width in the bottom photo is about 500 ns. The ac signal voltage in both cases is the same, 260 mv. An integration time of 600 μs was used for this measurement.

If the injected minority carriers were not recombined completely during the short injection pulse applied (50 ns), the ac signal should have been lower than that of the wider injection pulse (500 ns). The same signal, in both cases, therefore, implies that during the 50 ns time period, all of the injected charge carriers were recombined. In order to determine the experimental accuracy, we measured the modulated ac signal as a function of integration time for a given injection pulse width, as shown in Figure 53. The top trace is for a signal measured with an integration time of 500 μs, the bottom trace, 520 μs. In both cases, the injection pulse width was



50 ns/div.

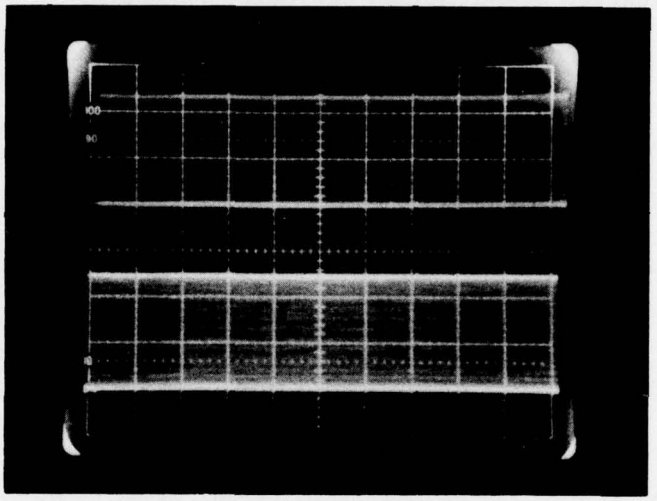
100 mv/div.
200 ns/div.



50 ns/div.

100 mv/div.
200 ns/div.

Figure 52. Output a-c Signal of an InSb CID as a Function of the Injection Pulse Width.



100 mv/div.

200 ns/div

Figure 53. Modulated a-c Signal As a Function of Integration Time for a Given Injection Pulse Width.

Integration Time for the Top Trace = 500 μs. Signal = 235 mv.

Integration Time for the Bottom Trace = 520 μs. Signal = 250 mv.

Injection Pulse Width for Both Cases = 50 ns.

set at 50 ns. As shown, the signal for the 500 μs integration time is 235 mv, and 250 mv for a 520 μs integration time. Thus, a change in integration time of about 5% causes the signal to change noticeably, indicating that the recombination measurements are quite accurate.

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